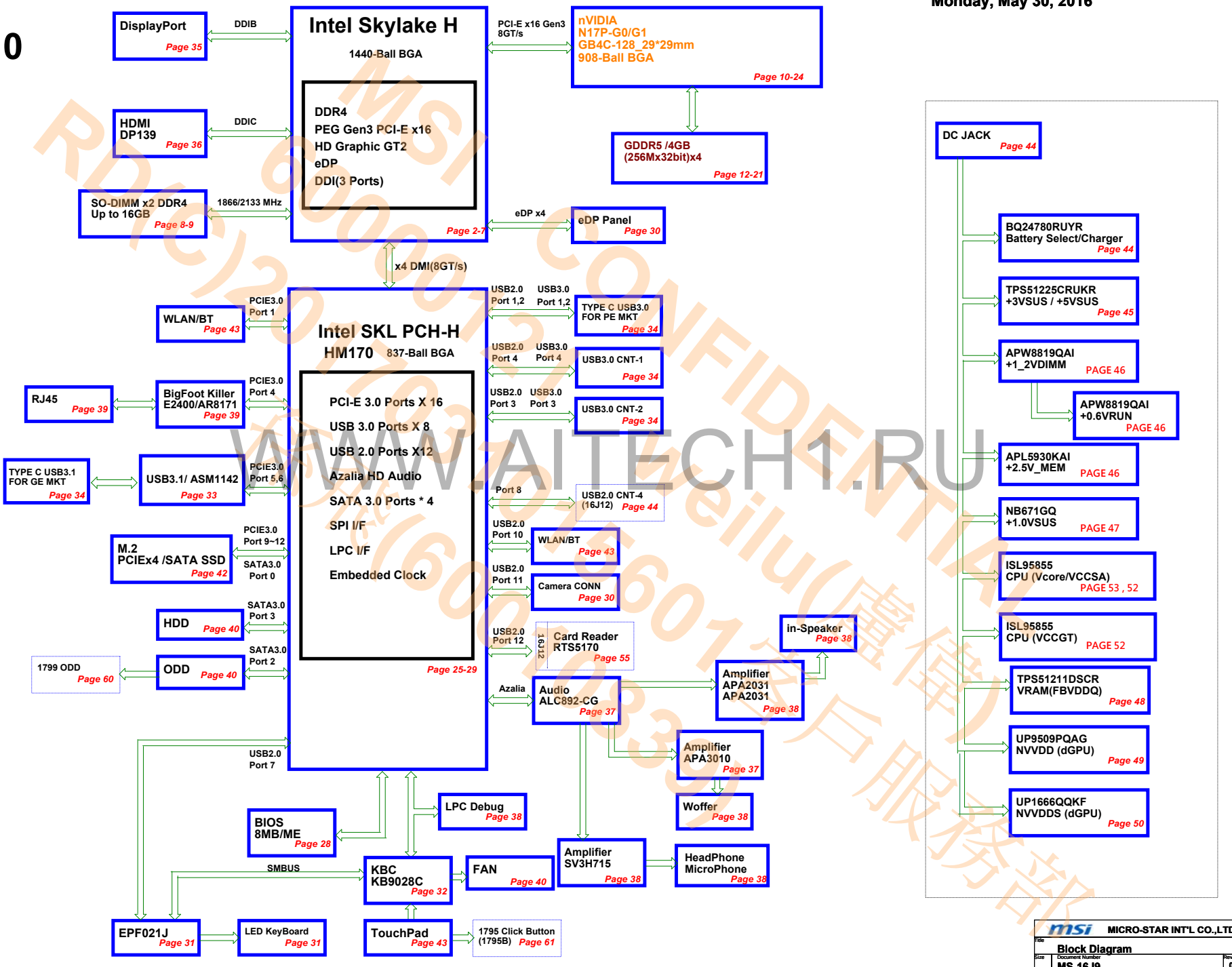
MS-16J9/MS-1799

Intel Skylake Mobile

Ver:10

Monday, May 30, 2016

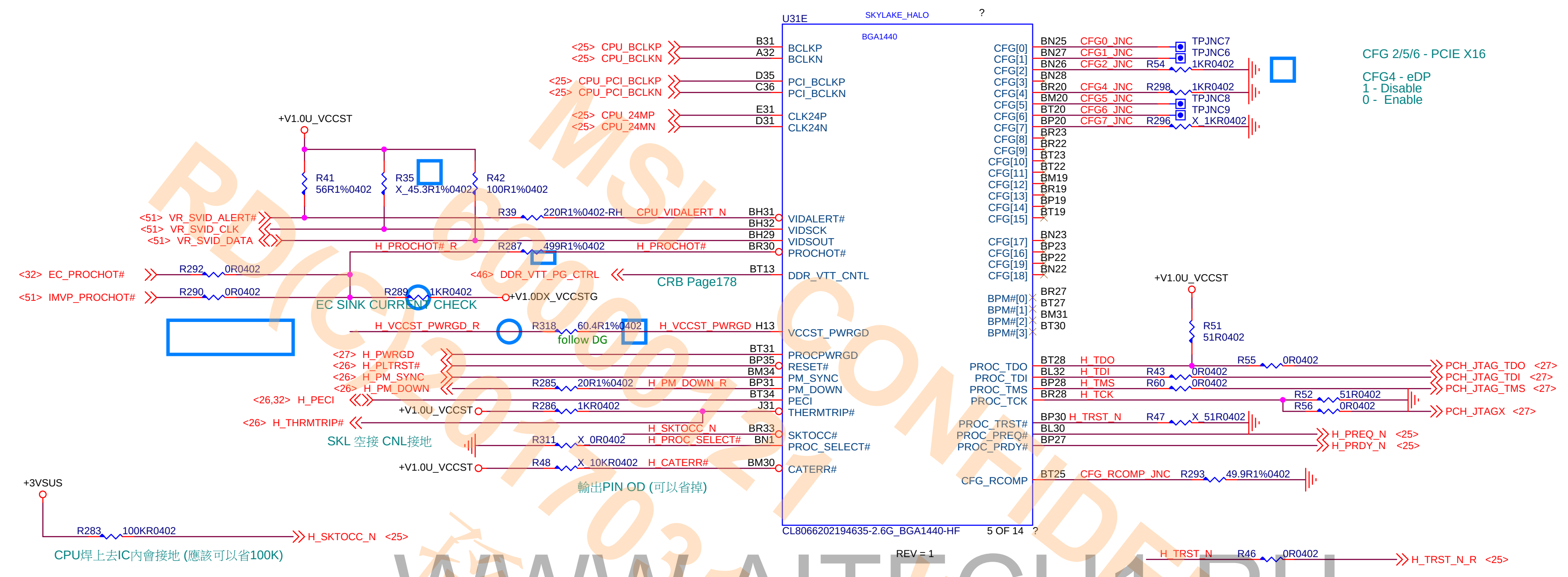


msi MICRO-STAR INT'L CO.,LTD.

Title: Block Diagram

Size | Document Number: MS-16J9 | Rev: 0A

Date: | Sheet 1 of 62



MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCIE Express * Static X16 Lane Numbering Reversal	
CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.

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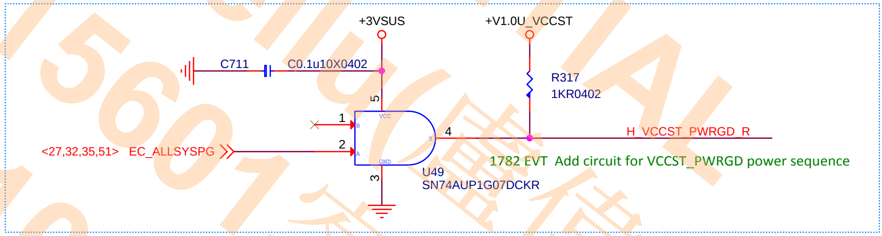
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*

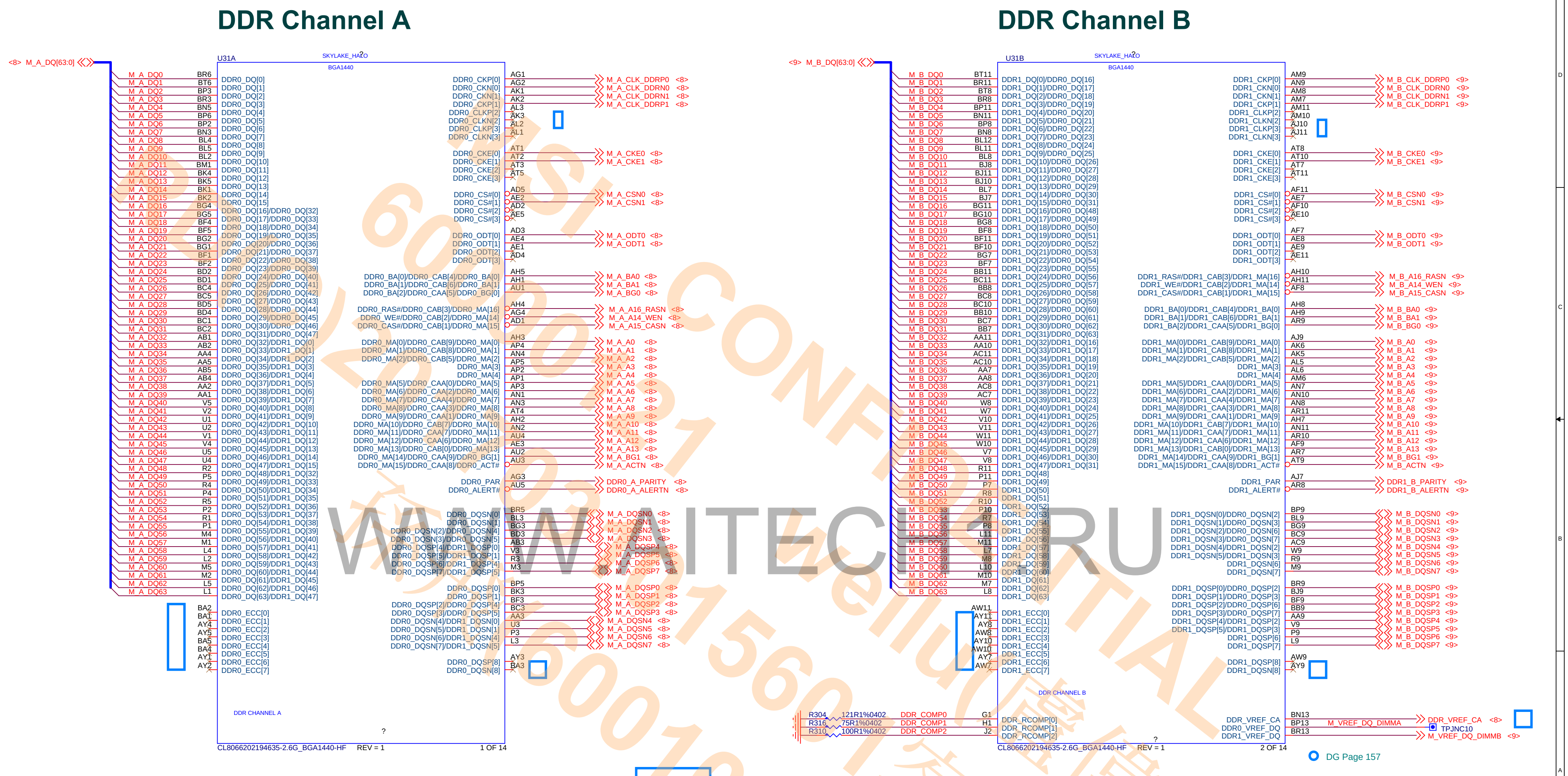


MICRO-STAR INT'L CO.,LTD.

Title: Skylake(HOST)

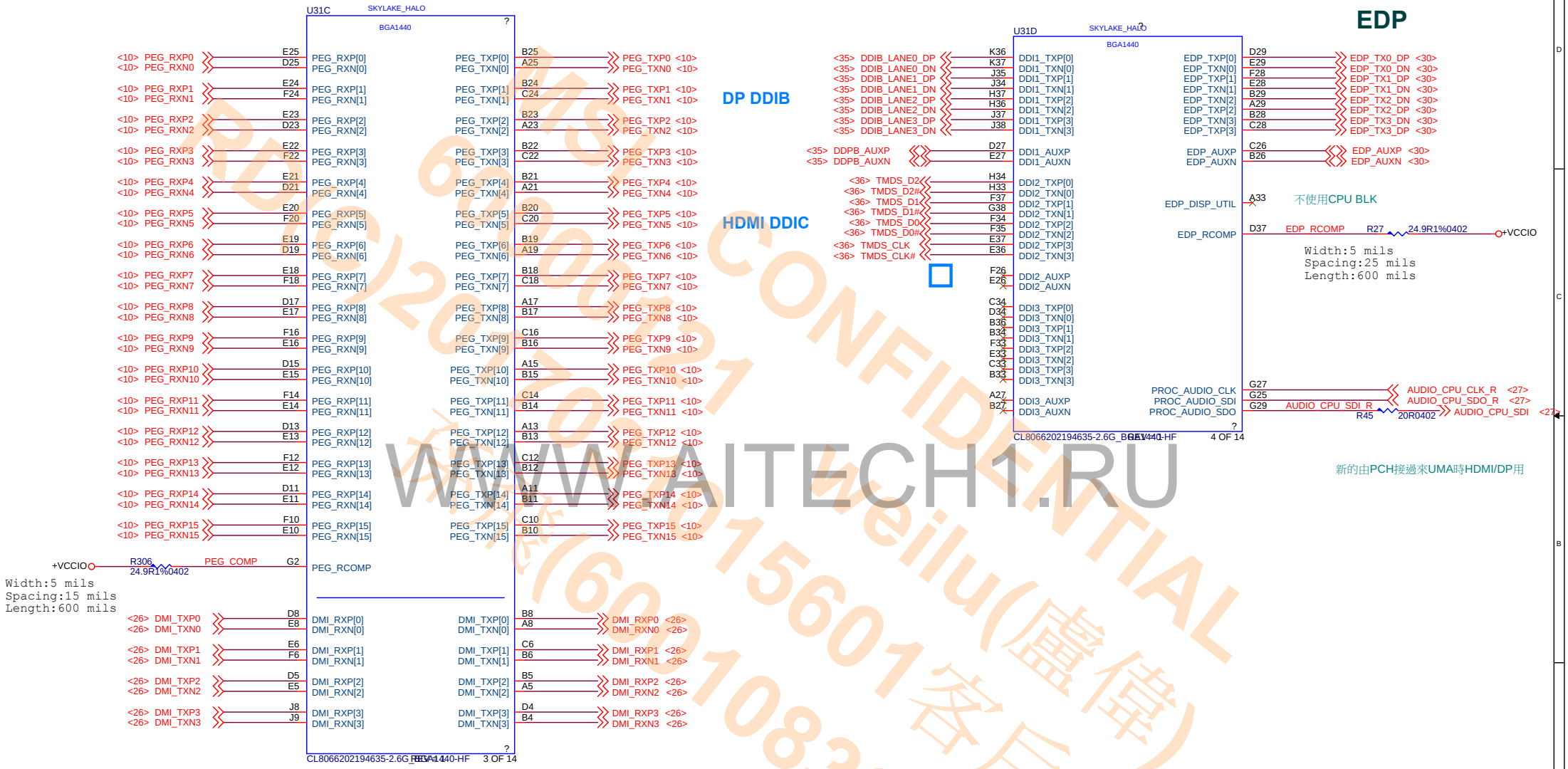
Size: A3 | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 2 of 62

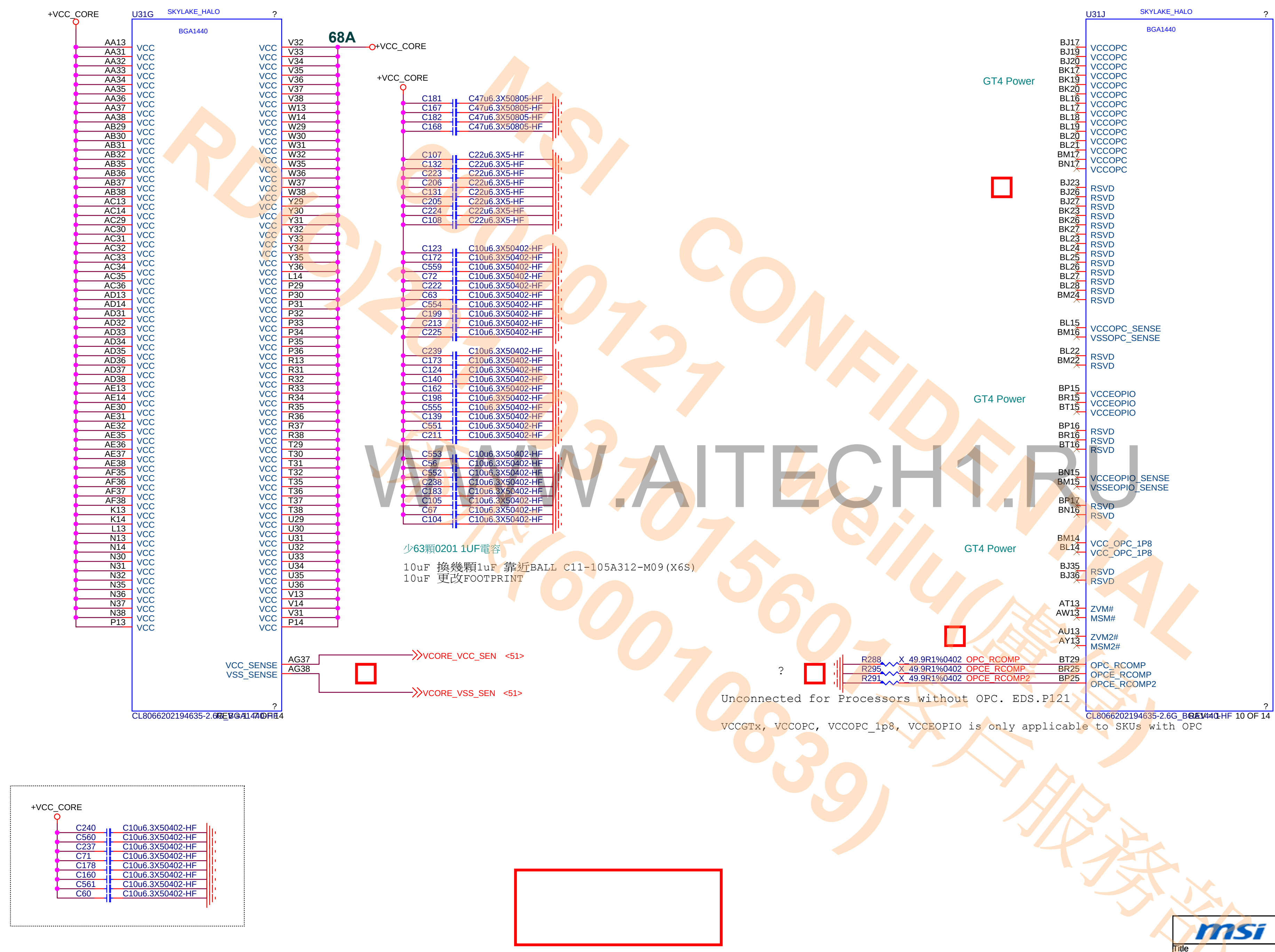


MICRO-STAR INT'L CO.,LTD.

Title	Skylake(DDR4)	
Size Custom	Document Number MS-16J9	Rev 0A
Date: Wednesday, July 27, 2016	Sheet 3 of 62	

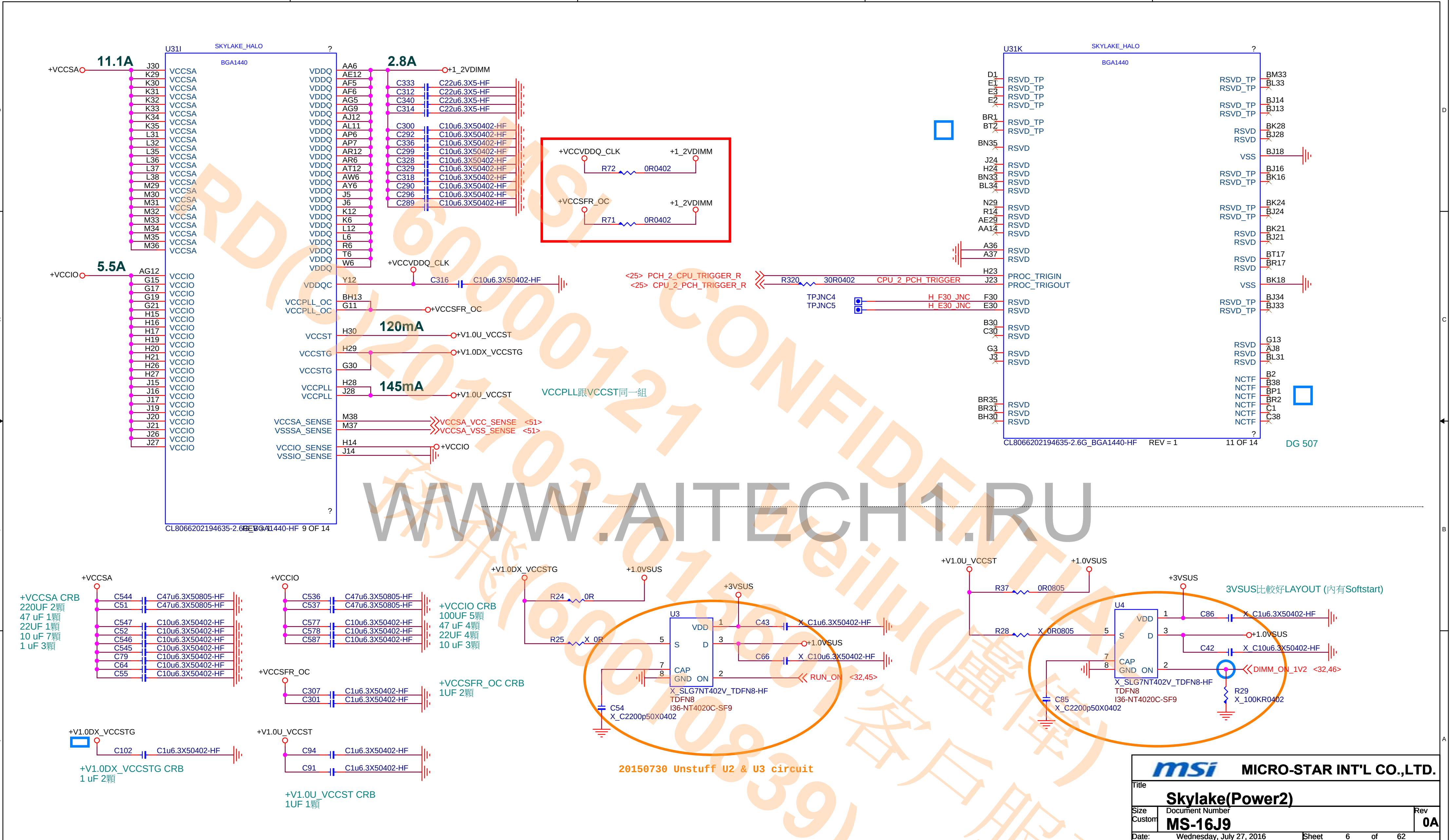


MICRO-STAR INT'L CO.,LTD.			
Title: Skylake(DMI/Display)			
Size: B	Document Number: MS-16J9		Rev: 0A
Date: Wednesday, July 27, 2016	Sheet 4 of 62		



MICRO-STAR INT'L CO.,LTD.

Title	Skylake(Power1)	
Size A3	Document Number MS-16J9	Rev 0A
Date: Wednesday, July 27, 2016	Sheet 5 of 62	

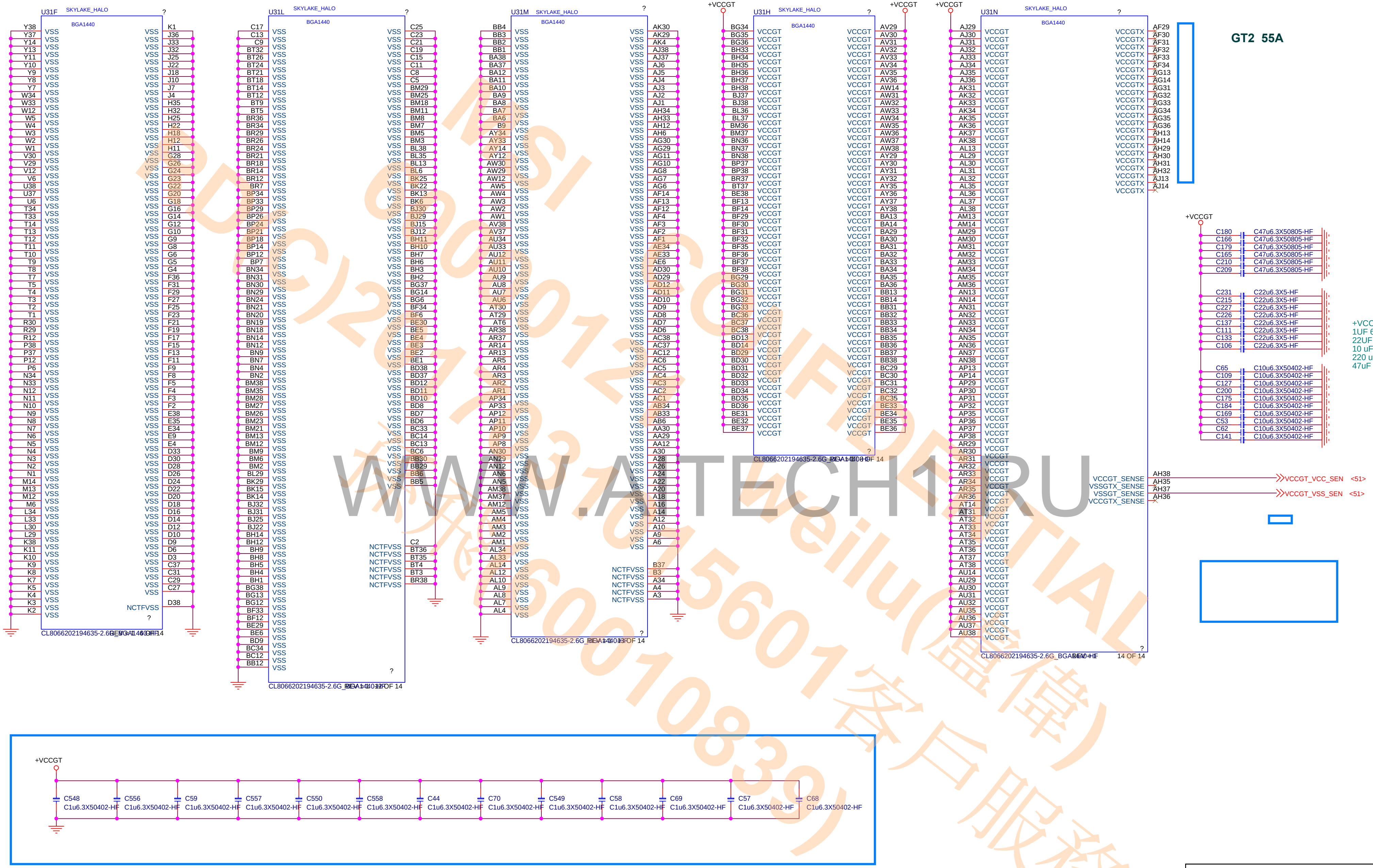


msi MICRO-STAR INT'L CO.,LTD.

Title: Skylake(Power2)

Size: Custom | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 6 of 62



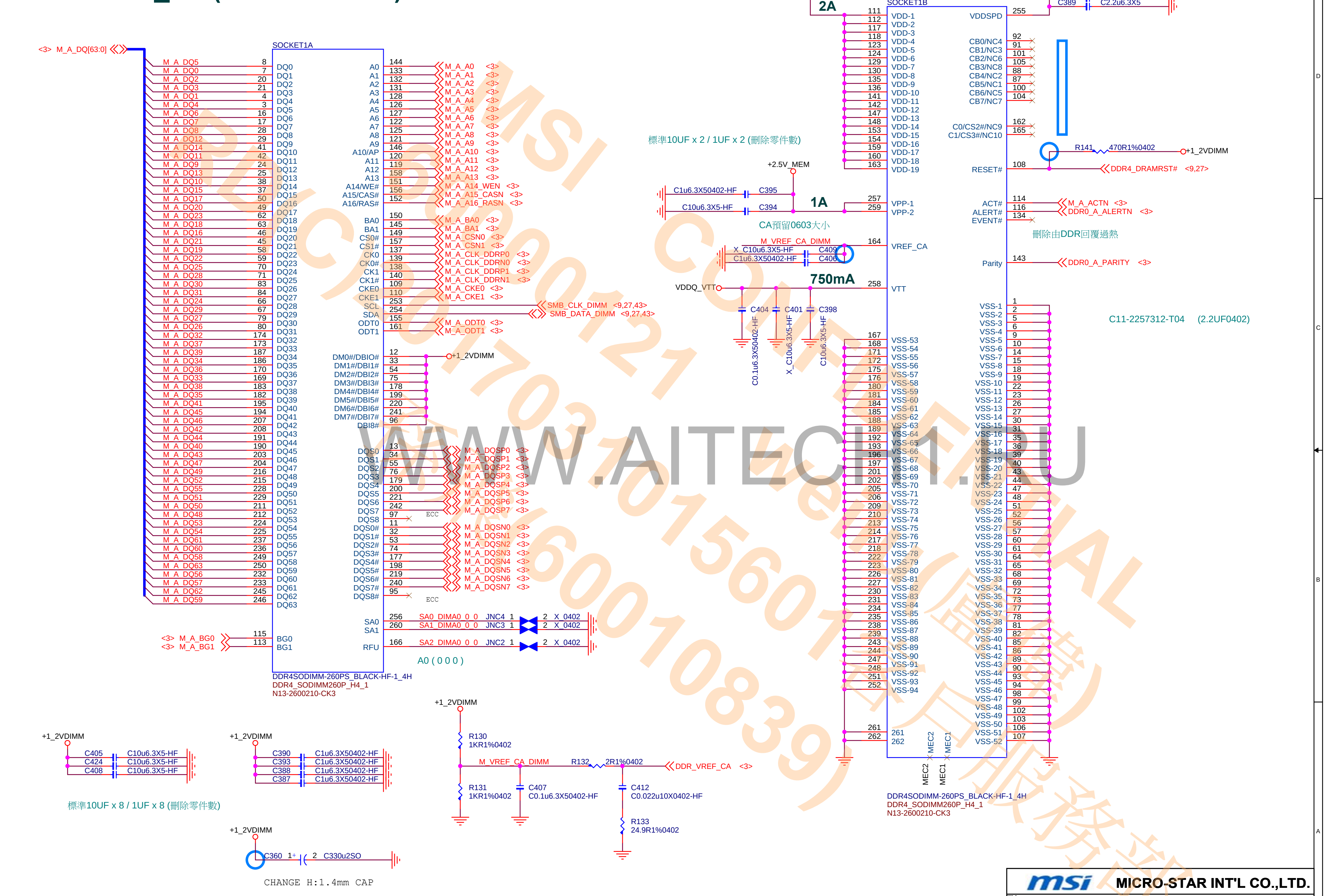
MICRO-STAR INT'L CO.,LTD.

Title: **Skylake(Power3)**

Size	Document Number	Rev
Custom	MS-16J9	0A

Date: Wednesday, July 27, 2016 Sheet 7 of 62

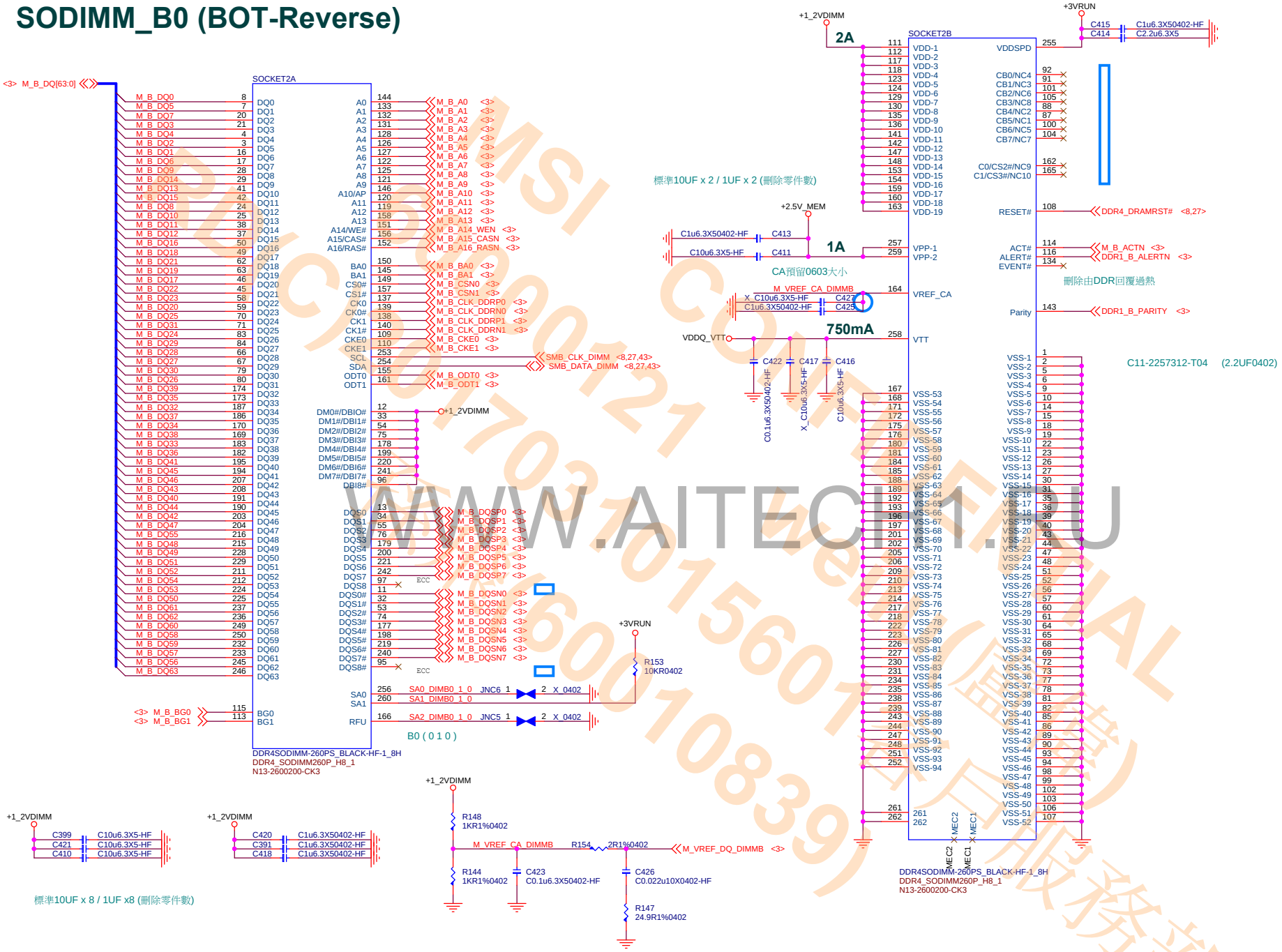
SODIMM_A0 (BOT-Reverse)



MICRO-STAR INT'L CO.,LTD.

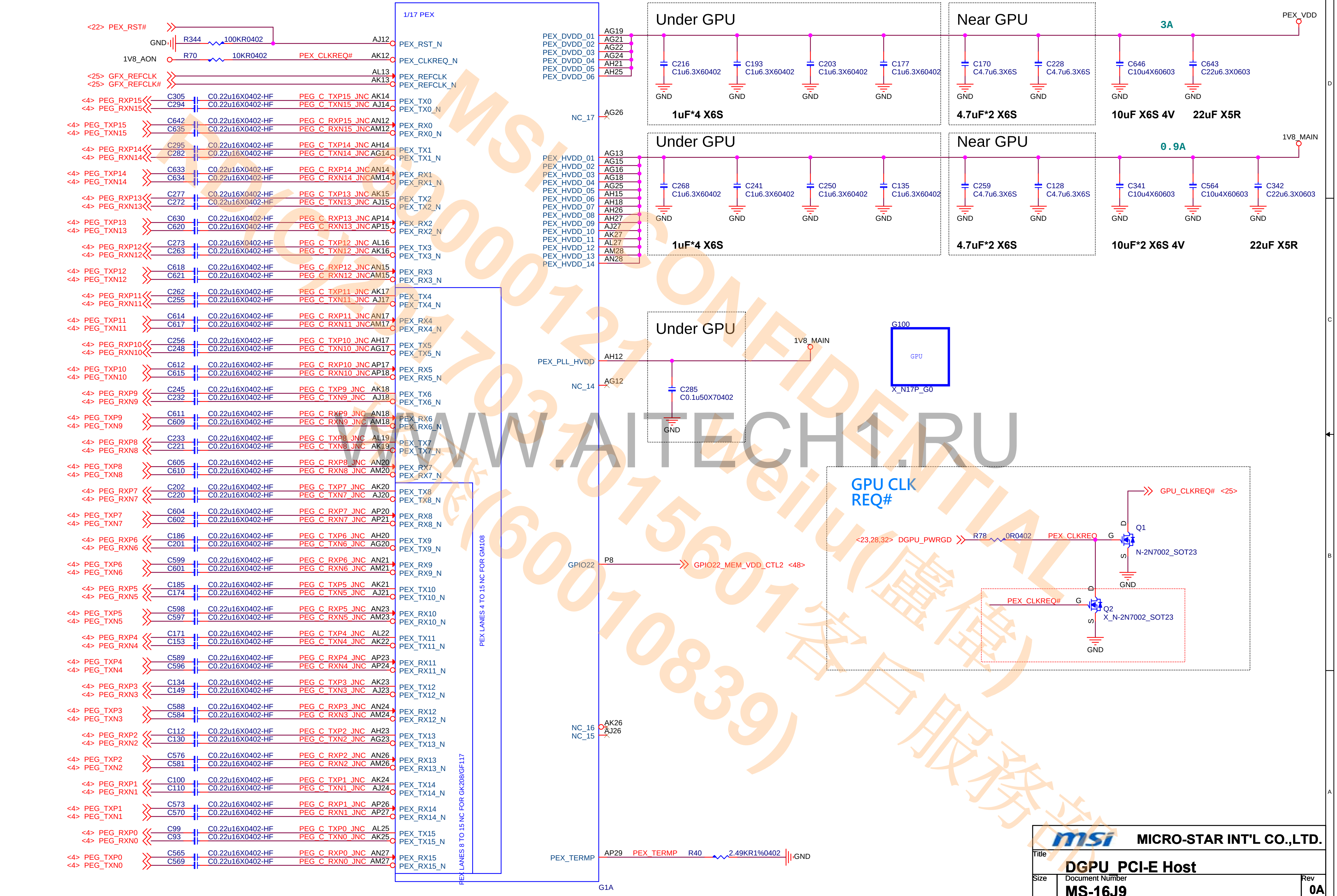
Title	DDR4_SODIMM_A0
Size Custom	Document Number MS-16J9
Rev	0A
Date:	Wednesday, July 27, 2016
Sheet	8 of 62

SODIMM_B0 (BOT-Reverse)



MICRO-STAR INT'L CO.,LTD.			
Title: DDR4_SODIMM_B0			
Size: Custom	Document Number: MS-16J9		Rev: 0A
Date: Wednesday, July 27, 2016	Sheet 9 of 62		

GPU PCI EXPRESS



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_PCI-E Host
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Date:	Wednesday, August 24, 2016
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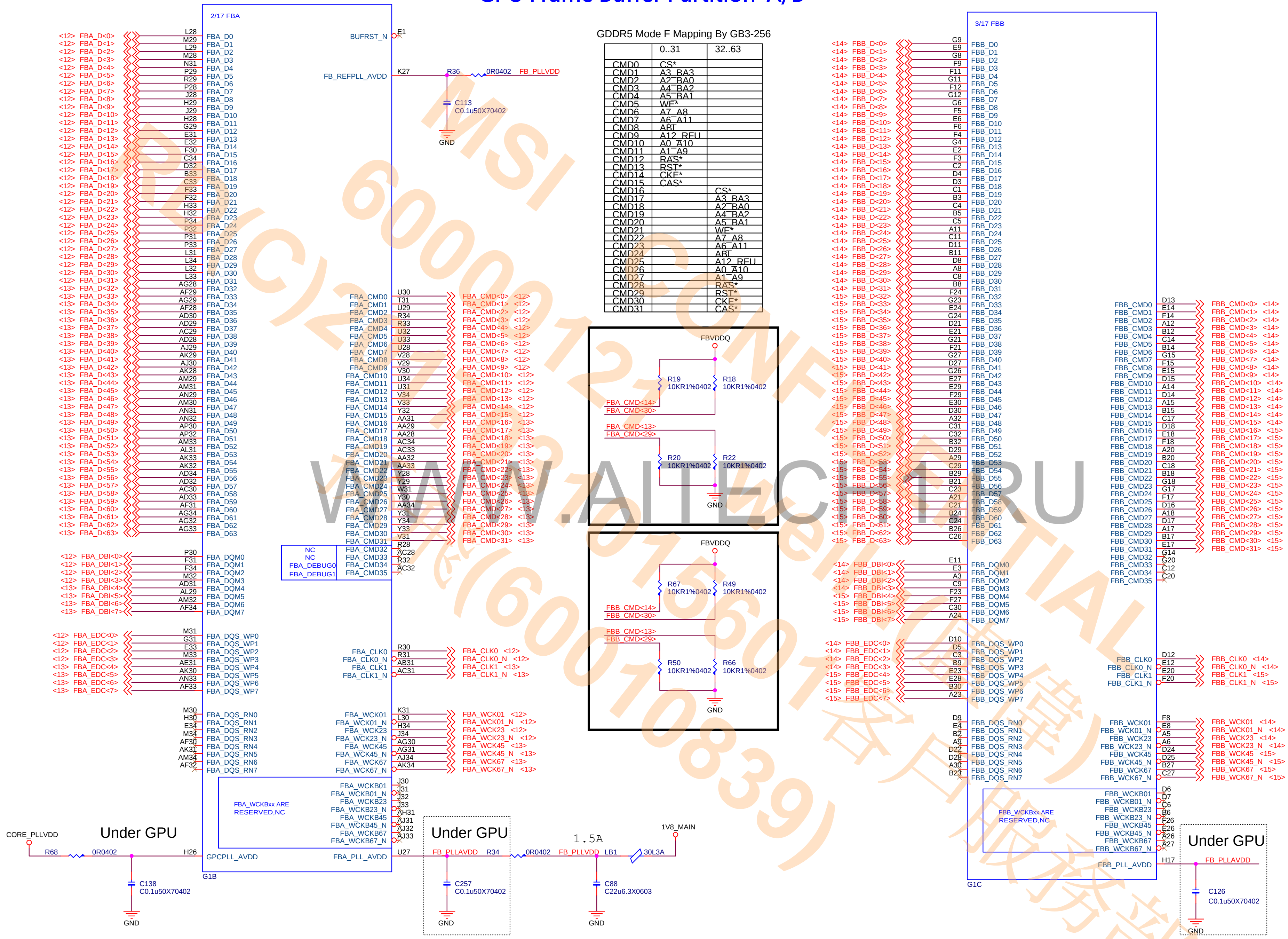
GPU Frame Buffer Partition A/B

GDDR5 Mode F Mapping By GB3-256

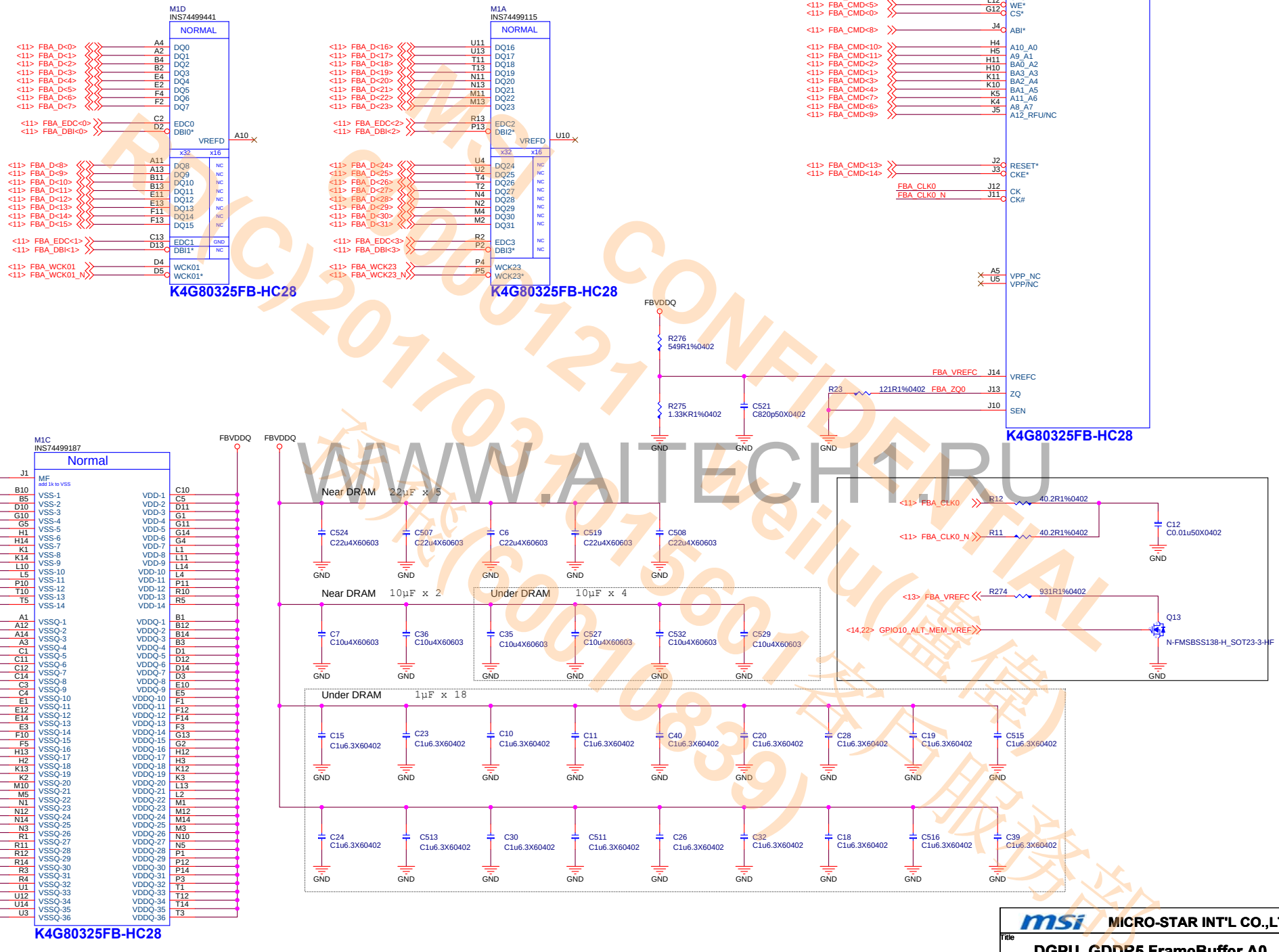
	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*



MICRO-STAR INT'L CO.,LTD.

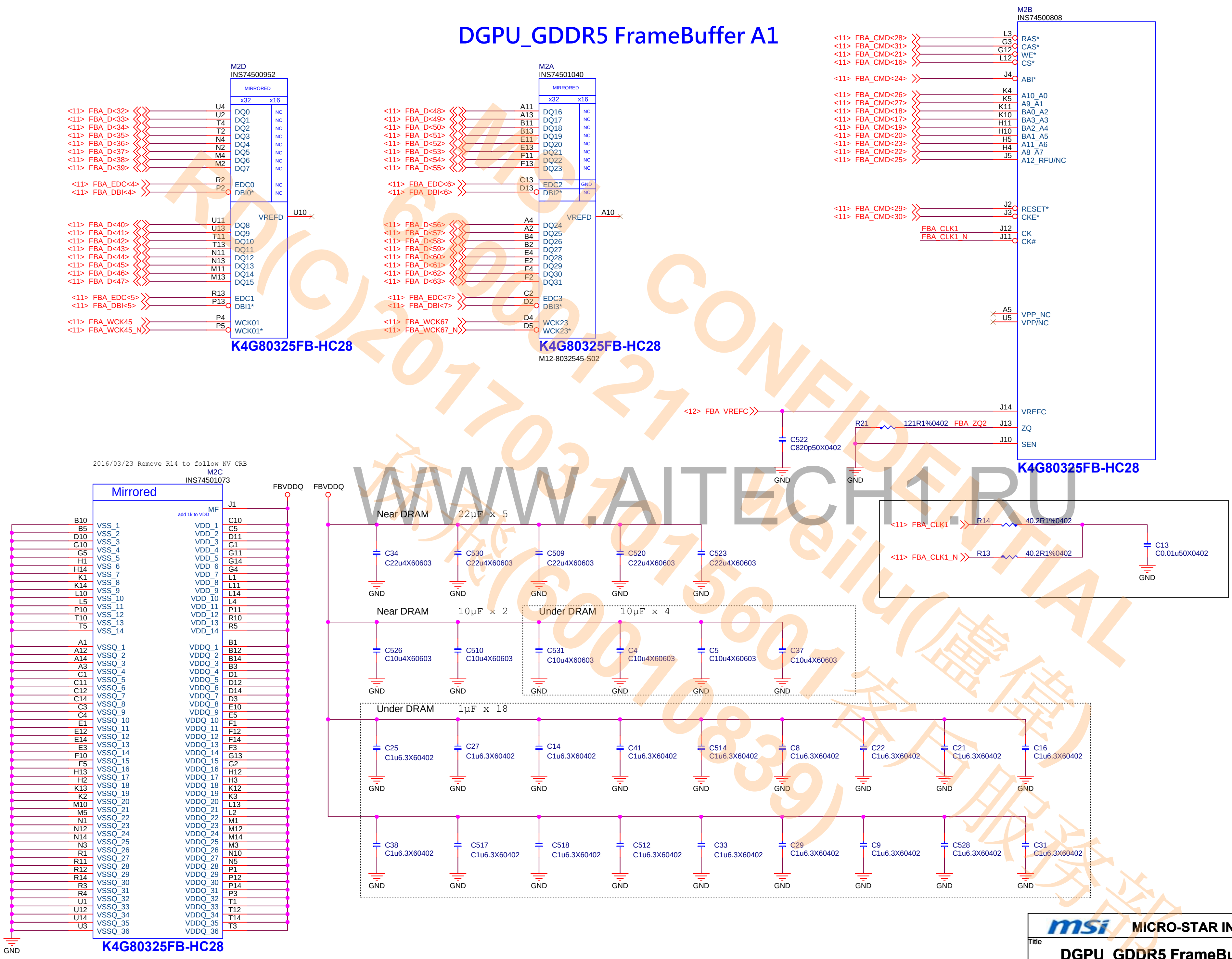
Title	DGPU_MEM IF A/B	
Size	Document Number MS-16J9	Rev 0A
Date: Wednesday, August 24, 2016	Sheet 11 of 62	

DGPU_GDDR5 FrameBuffer A0



MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer A0			
Size	Document Number: MS-16J9		Rev: 0A
Date: Wednesday, August 03, 2016	Sheet 12 of 62		

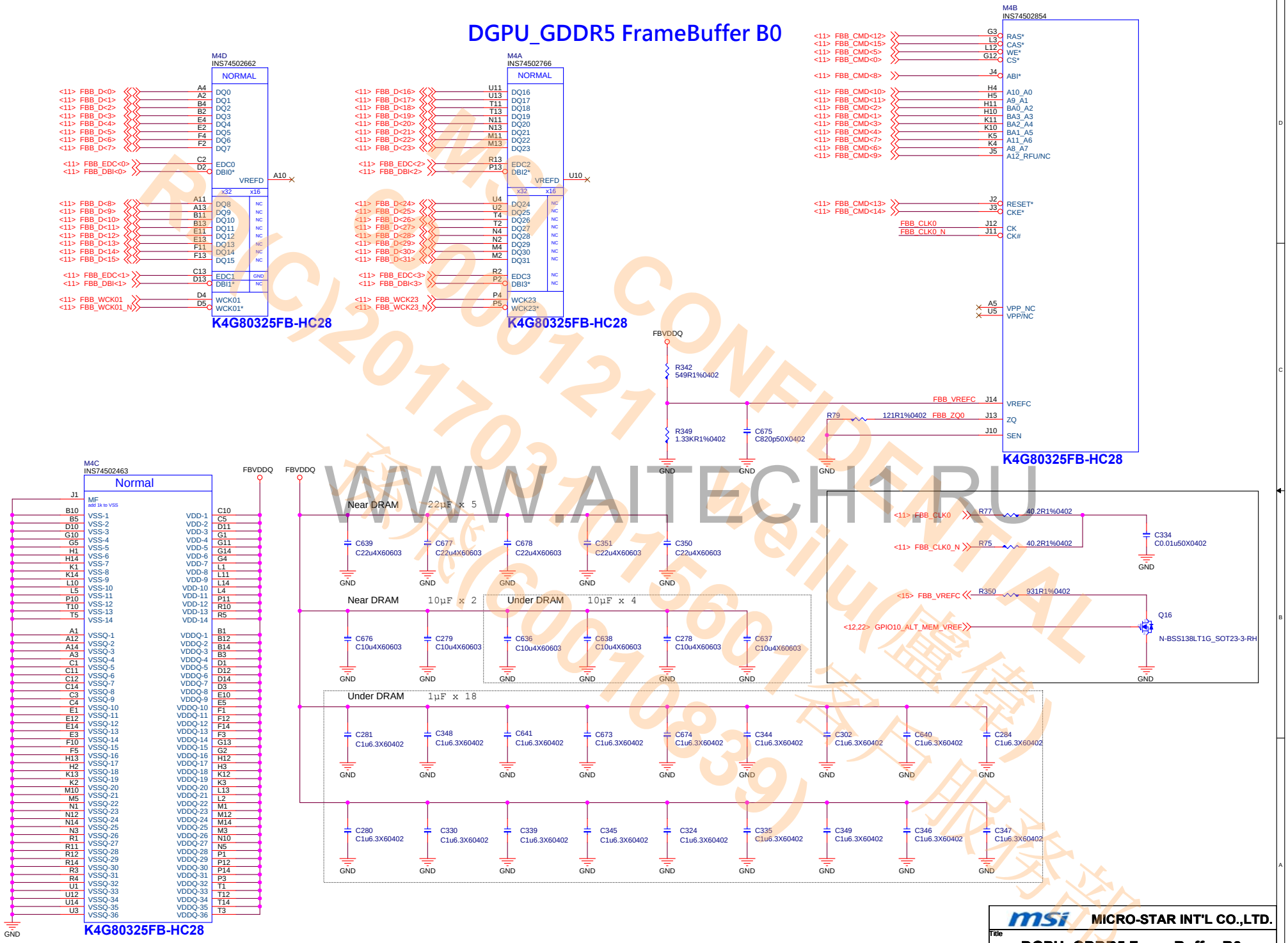
DGPU_GDDR5 FrameBuffer A1



MICRO-STAR INT'L CO.,LTD.

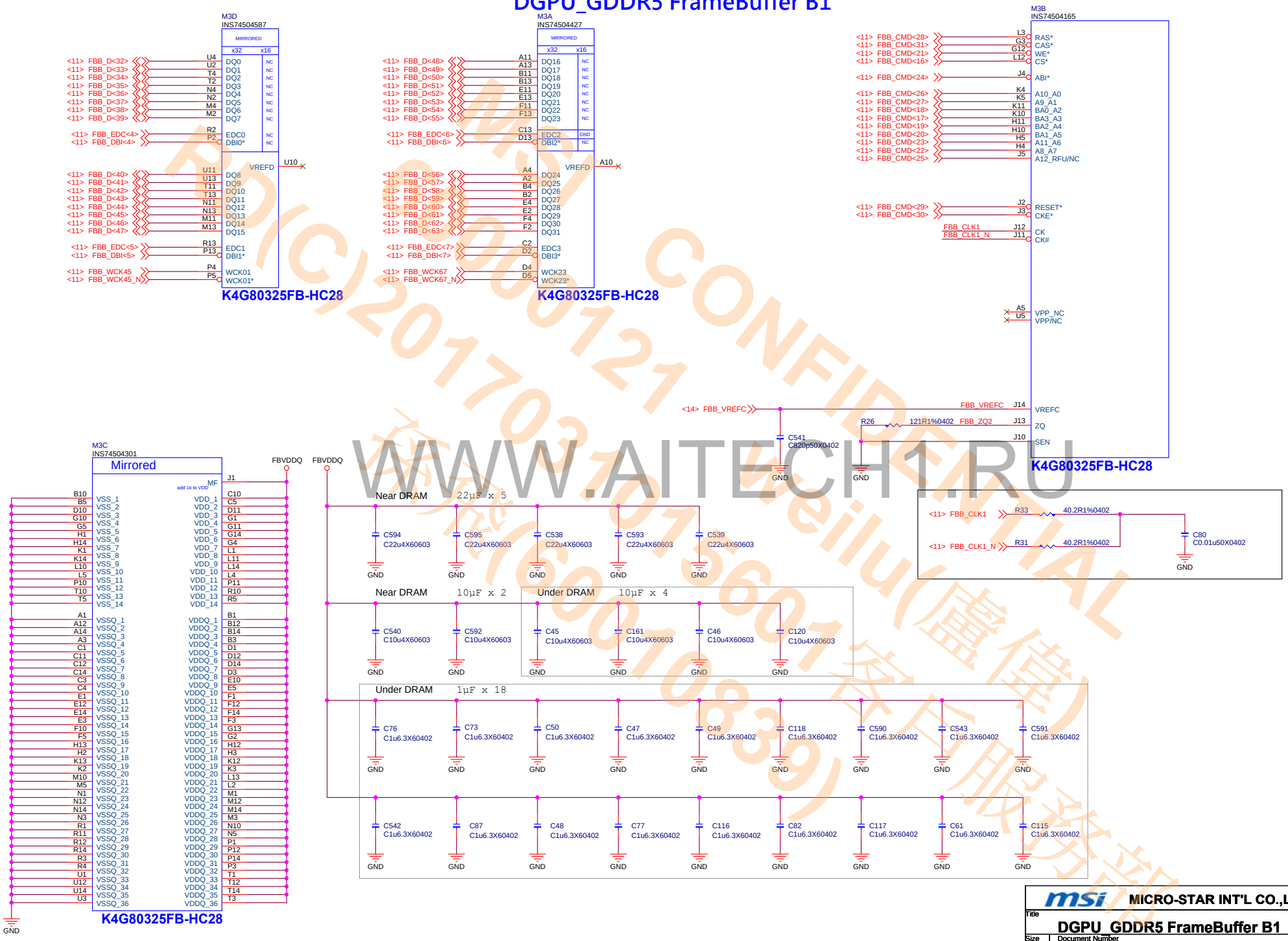
Title	DGPU_GDDR5 FrameBuffer A1	
Size	Document Number: MS-16J9	Rev: 0A
Date: Wednesday, August 03, 2016	Sheet 13 of 62	

DGPU_GDDR5 FrameBuffer B0

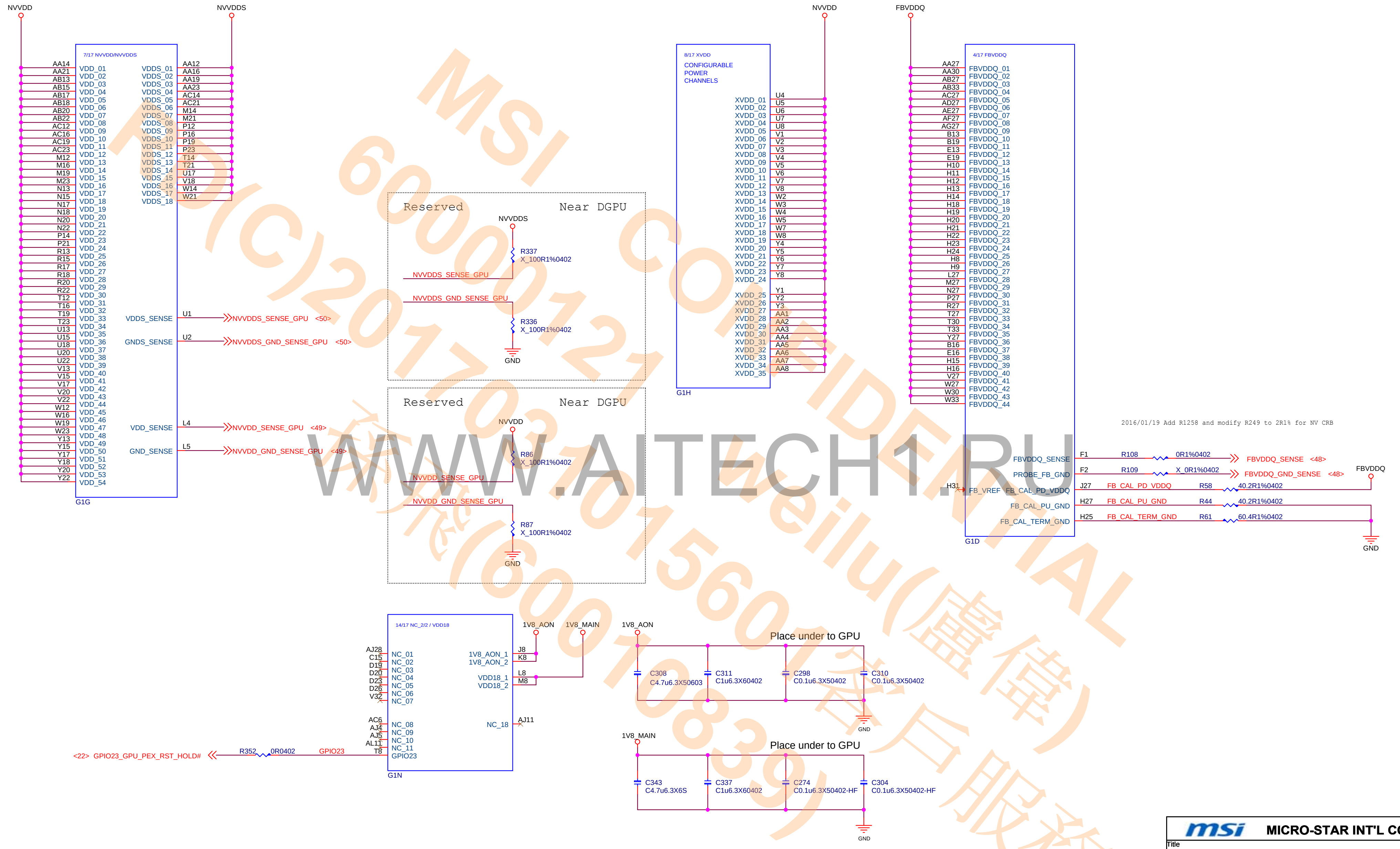


MICRO-STAR INT'L CO.,LTD.			
Title: DGPU_GDDR5 FrameBuffer B0			
Size	Document Number: MS-16J9		Rev: 0A
Date: Wednesday, August 03, 2016	Sheet 14 of 62		

DGPU_GDDR5 FrameBuffer B1



GPU NVVDD, FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title	DGPU NVVDD, FBVDDQ
Size / Document Number	MS-16J9
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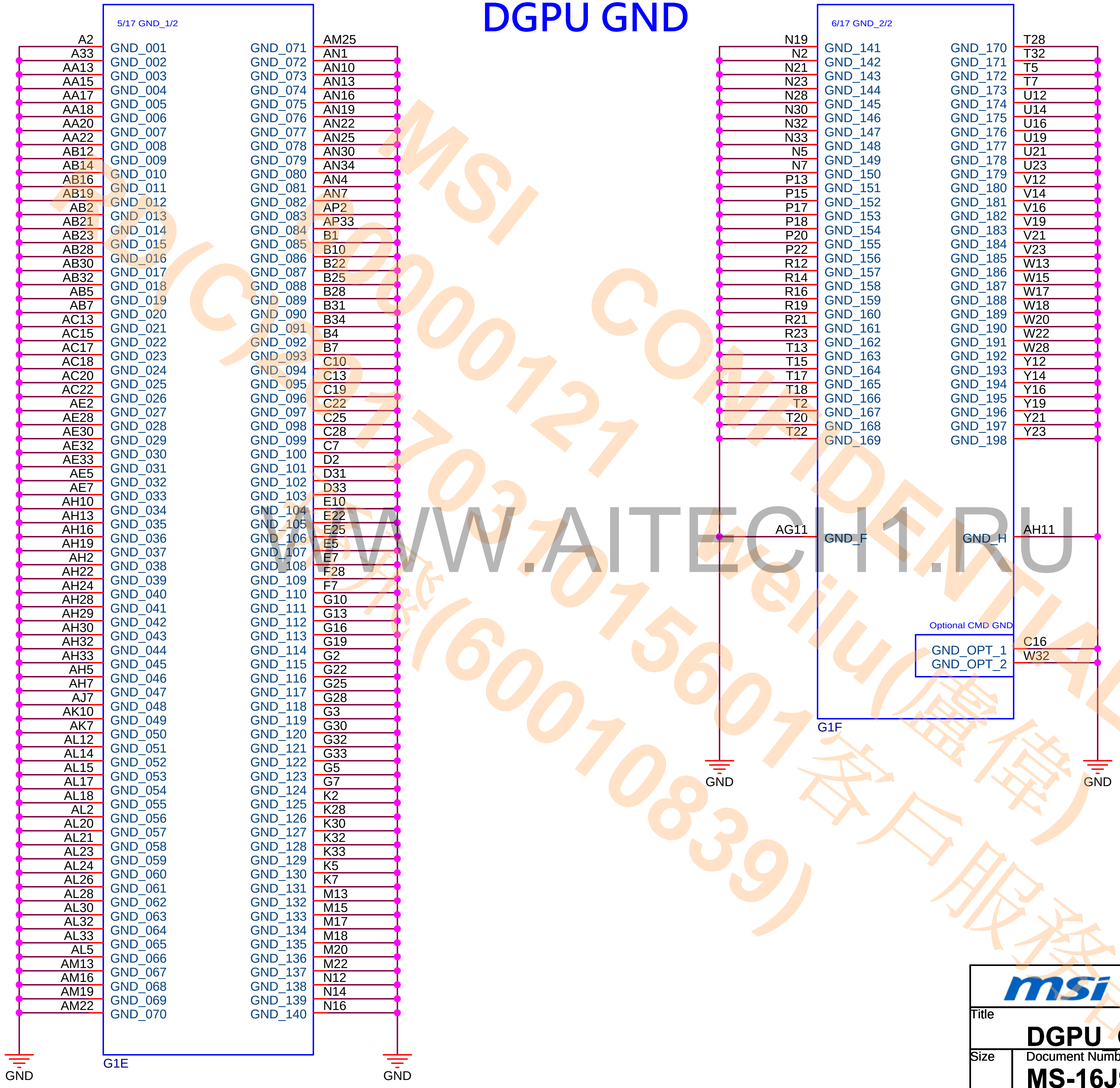
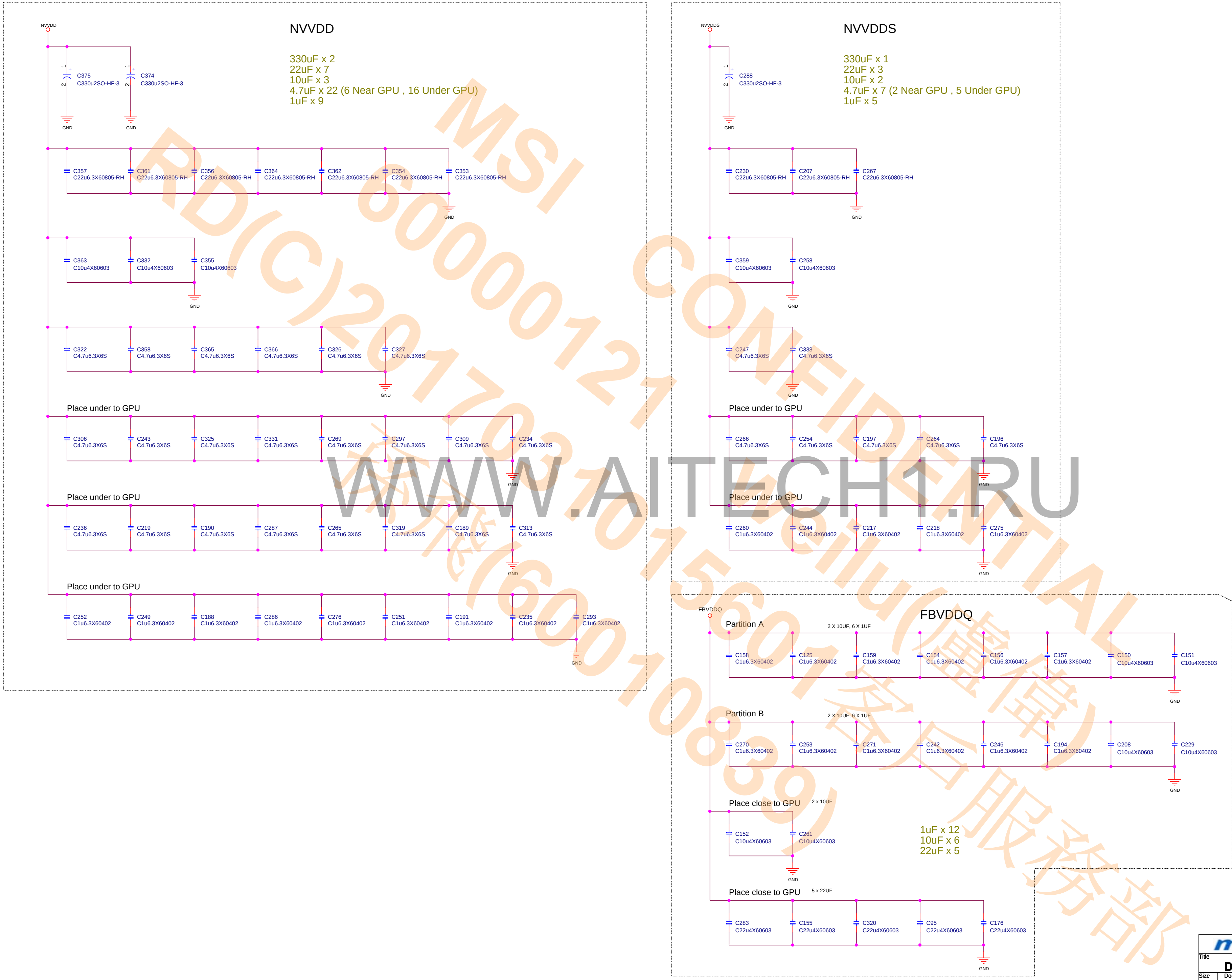
DGPU GND



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GND	
Size	Document Number MS-16J9	Rev 0A
Date: Wednesday, August 24, 2016	Sheet 17 of 62	

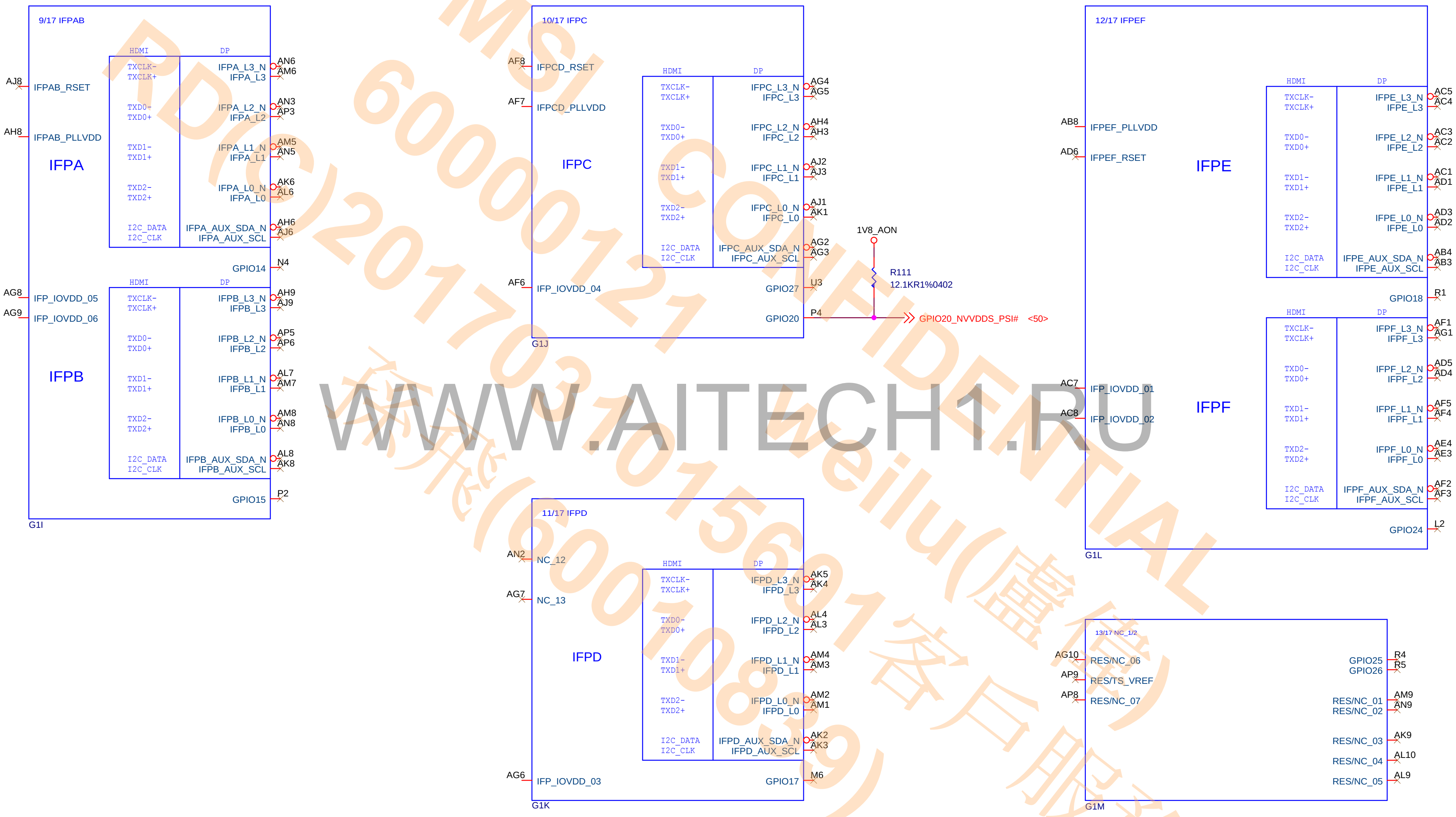
GPU DECOUPLING



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_GPU DECOUPLING	
Size	Document Number MS-16J9	Rev 0A
Date: Wednesday, July 27, 2016	Sheet 18 of 62	

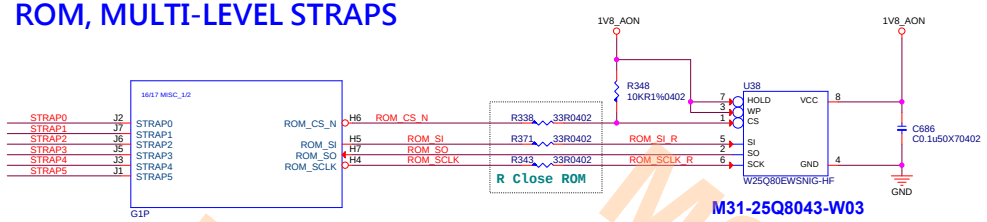
DACA,Display IF



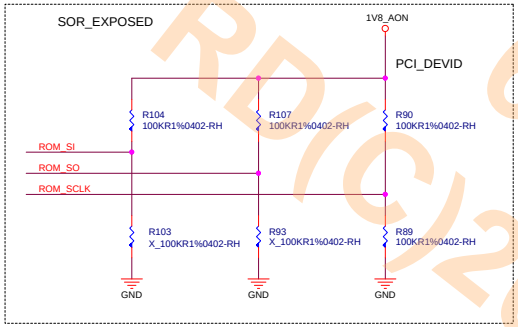
MICRO-STAR INT'L CO.,LTD.

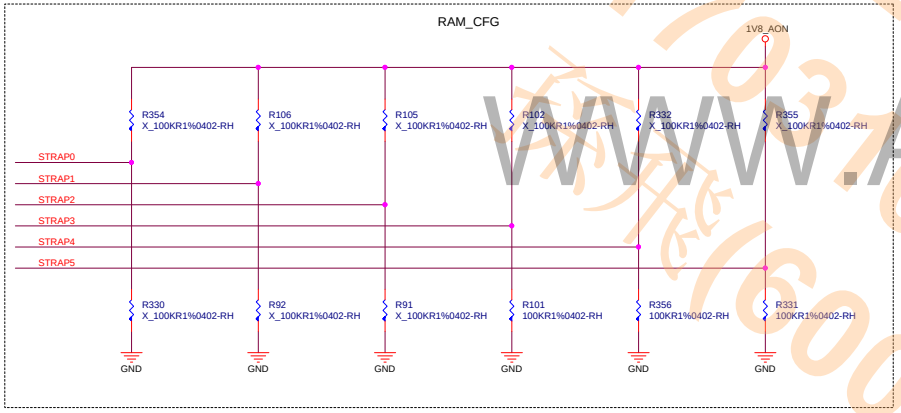
Title	DGPU_DACA,Display IF	
Size	Document Number MS-16J9	Rev 0A
Date: Wednesday, August 24, 2016	Sheet 19 of 62	

ROM, MULTI-LEVEL STRAPS



M31-25Q8043-W03





ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	R330.R92.R91
L	L	H	0x1 Micron: MT51J256M32HF-70:A	R354.R92.R91
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R330.R106.R91
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R354.R106.R91
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R354.R106.R105
L	L	M	0x8 Micron: EDW032BABG-70-F:A	R330.R92.R105.R91
L	M	L		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

MICRO-STAR INT'L CO.,LTD.		
Title: DGPU_ROM,HW Straps		
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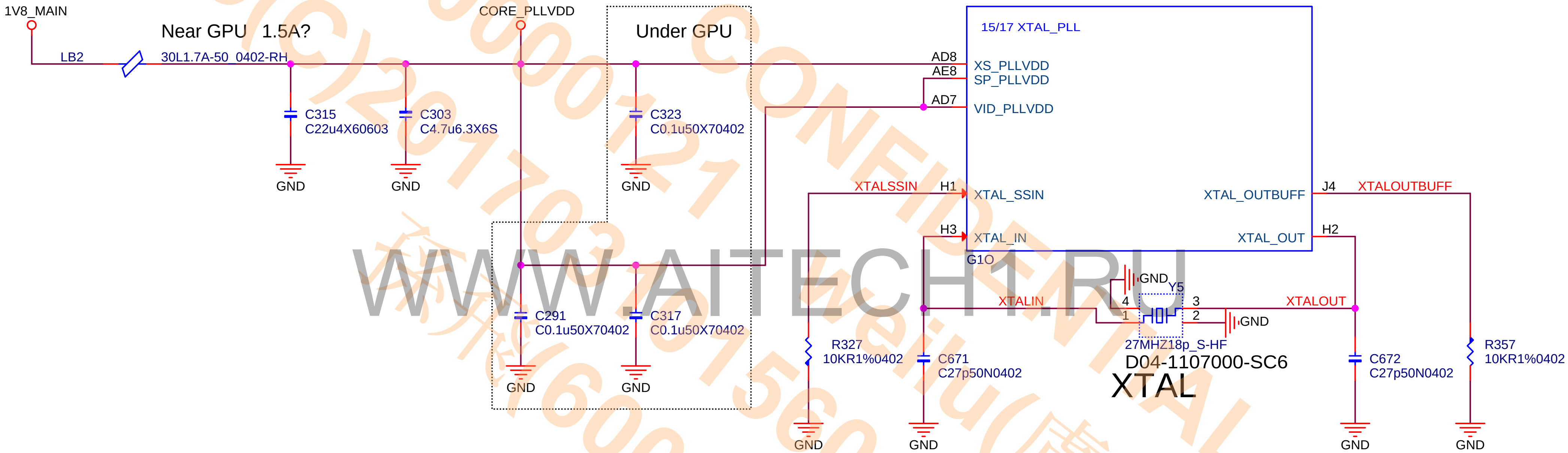
DGPU XTAL



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_XTAL
Size	Document Number: MS-16J9
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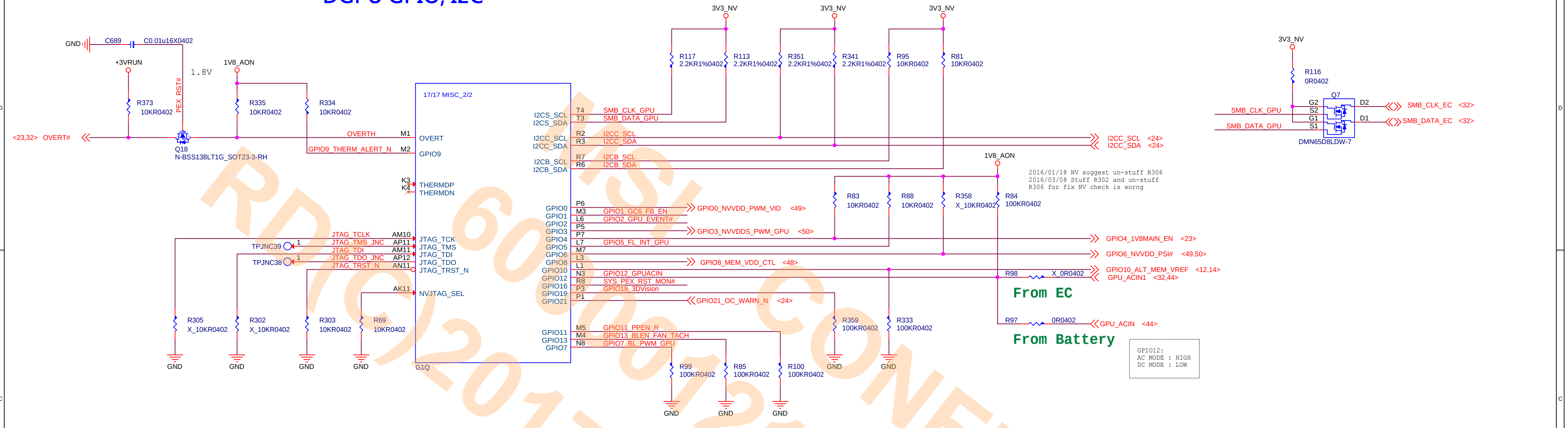
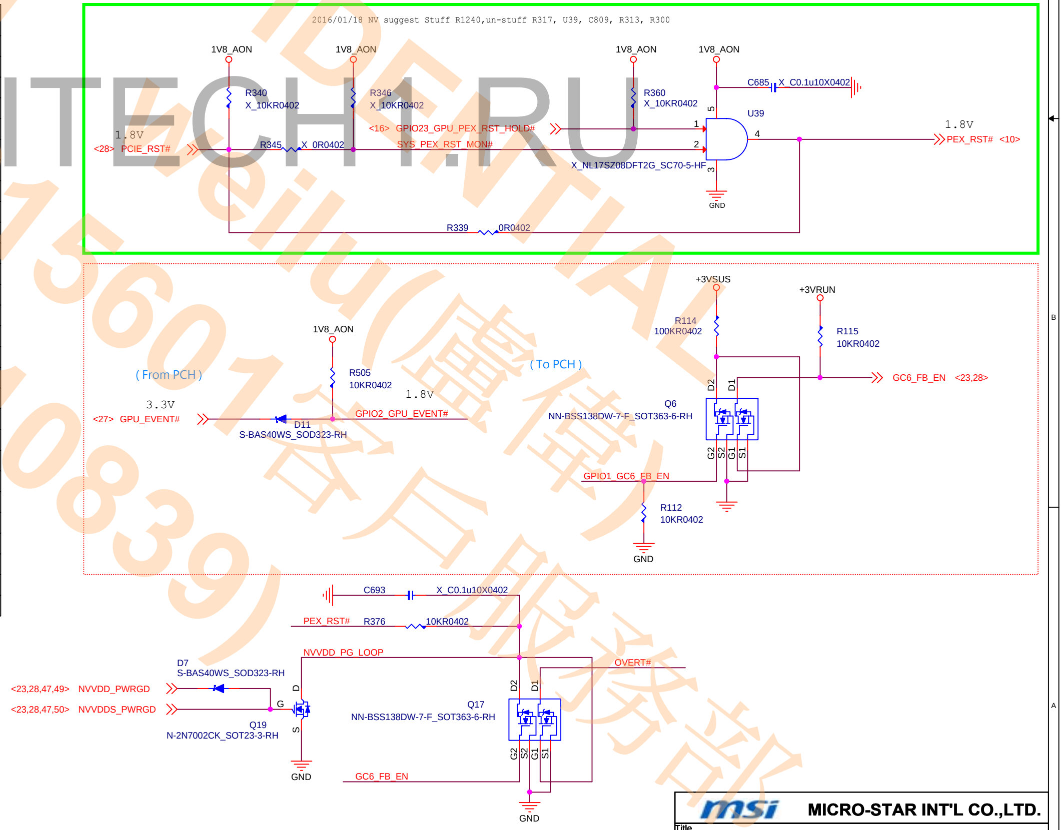
DGPU GPIO, I2C



Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	O	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	



msi	MICRO-STAR INT'L CO.,LTD.
Title	DGPU_GPIO,I2C
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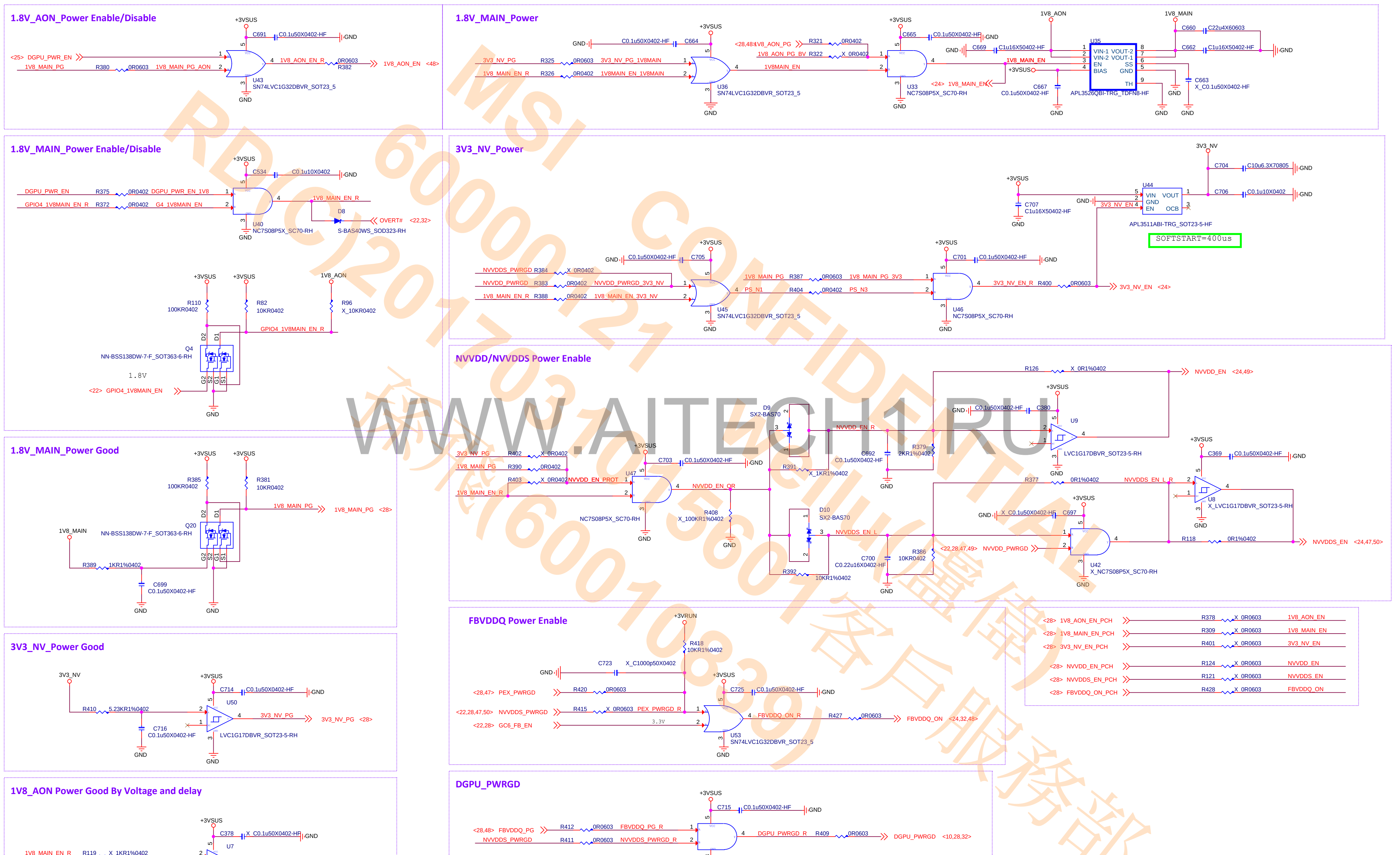
nVIDIA Power Sequence Control

Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

Power Off=NVVDDS/PEX_VDD/FBVDDQ(無先後順序)->NVVDD/NV3V3(可同時掉)->1V8_MAIN->1V8_AON



MICRO-STAR INT'L CO.,LTD.

Title	DGPU_Power Sequence
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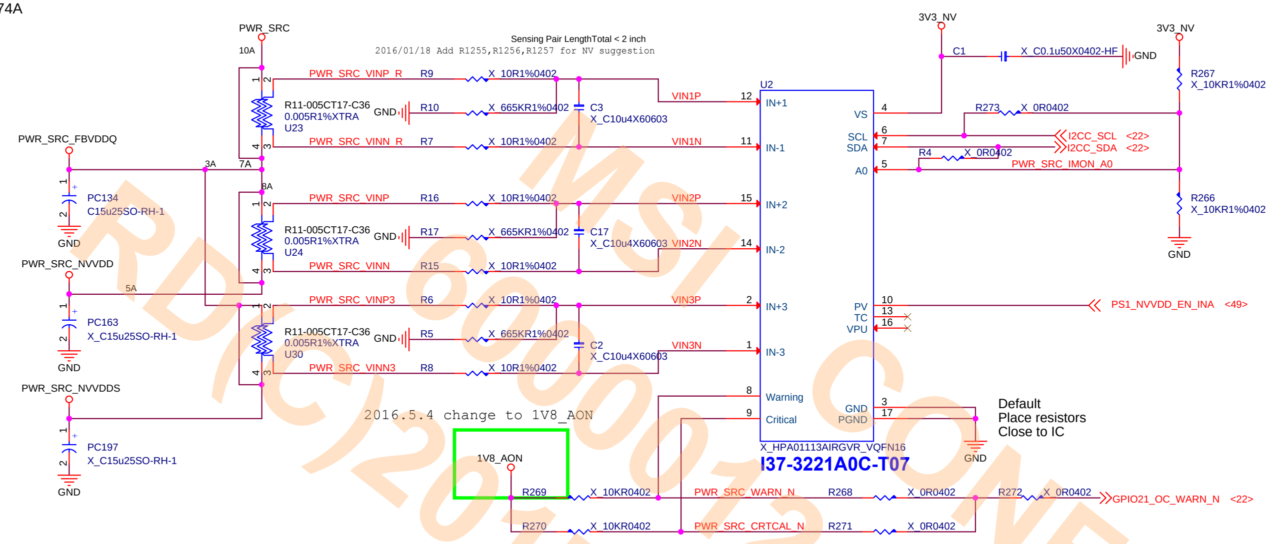
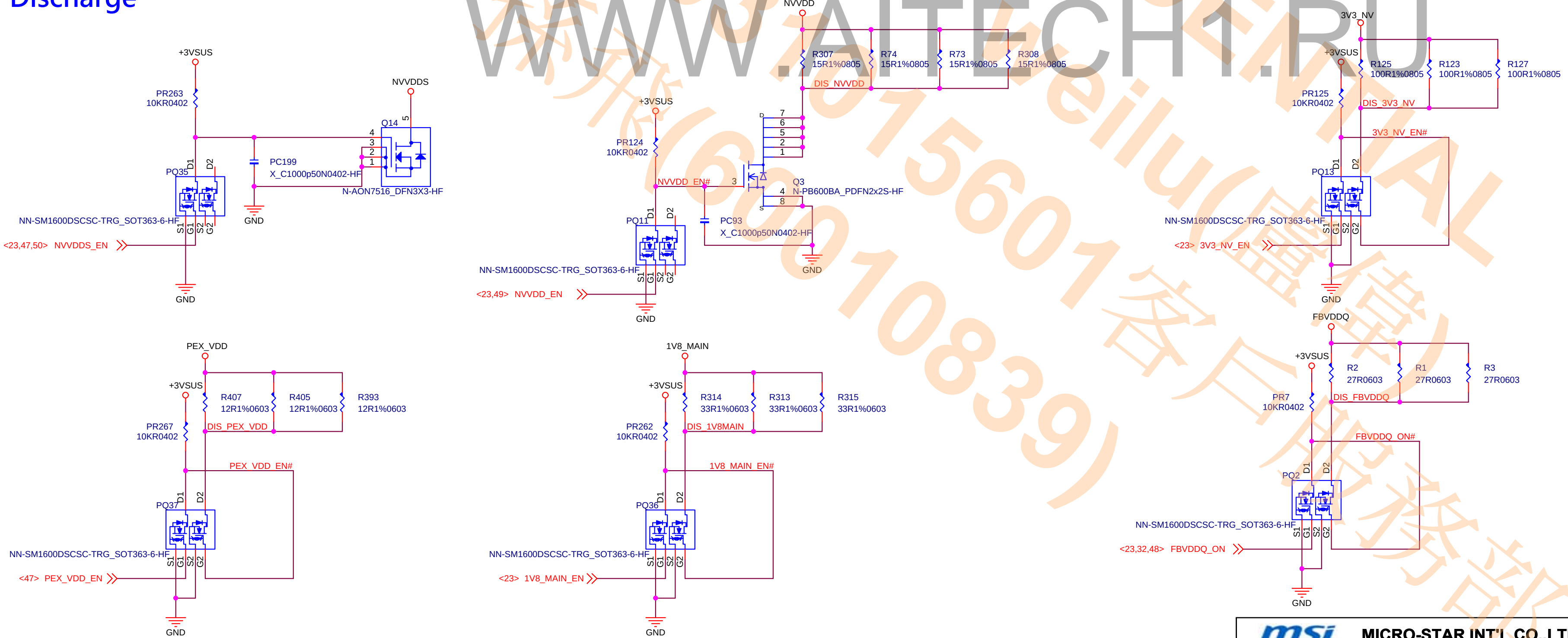
EDP Design Guide:
N17E-G1(90W)
NVVDD : 58A ; Peak 136A
NVVDDS : 28A ; Peak 74A
1.8V : 0.9A
PEX_VDD : 3A
FBVDDQ : 16A

DGPU_Power Control/Discharge



Discharge



MICRO-STAR INT'L CO.,LTD.

Title: DGPU_Discharge

Size | Document Number: MS-16J9 | Rev: 0A

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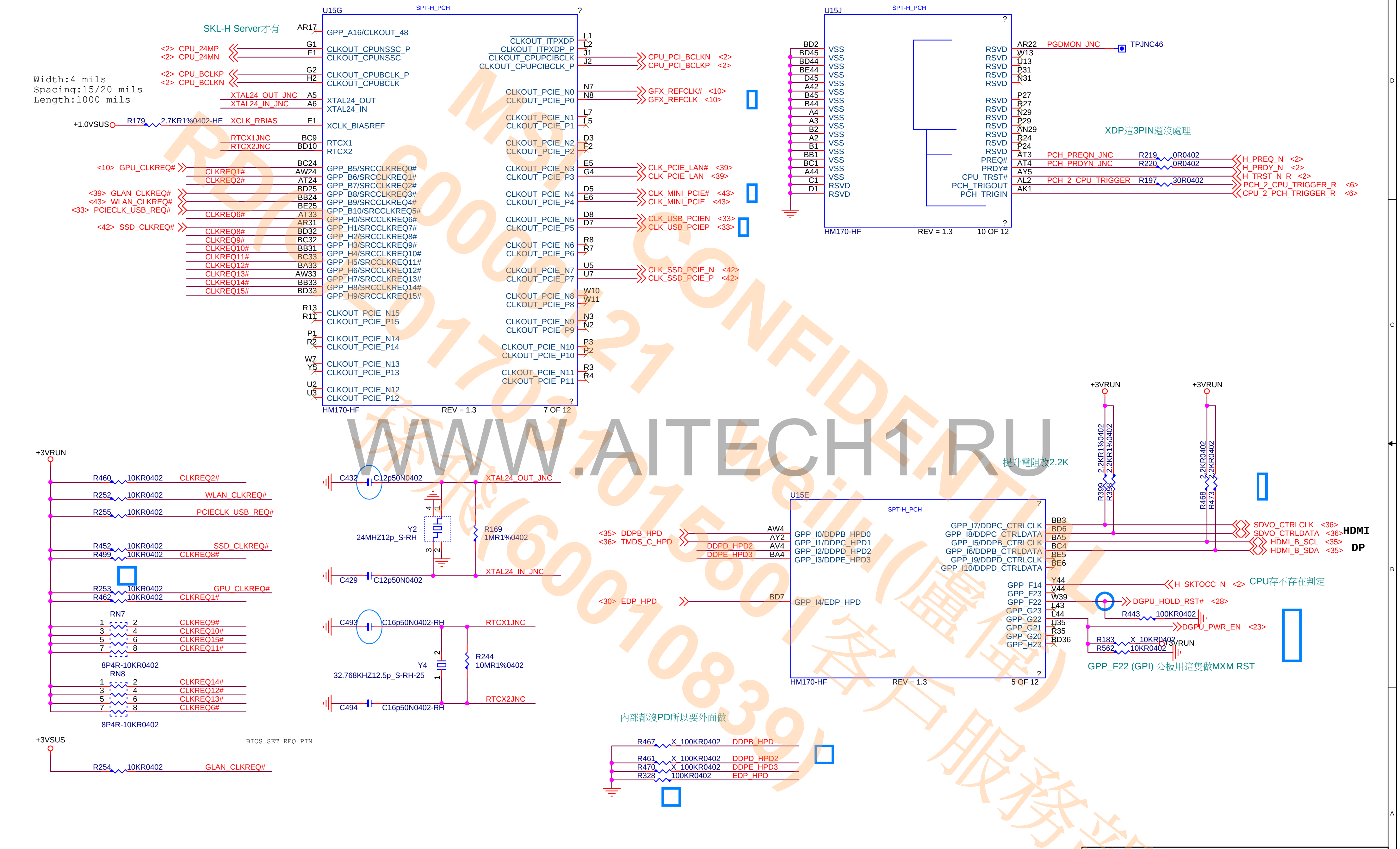

MICRO-STAR INT'L CO.,LTD.

Title: **PCH_1(CLK/DDI)**

Size	Document Number	Rev
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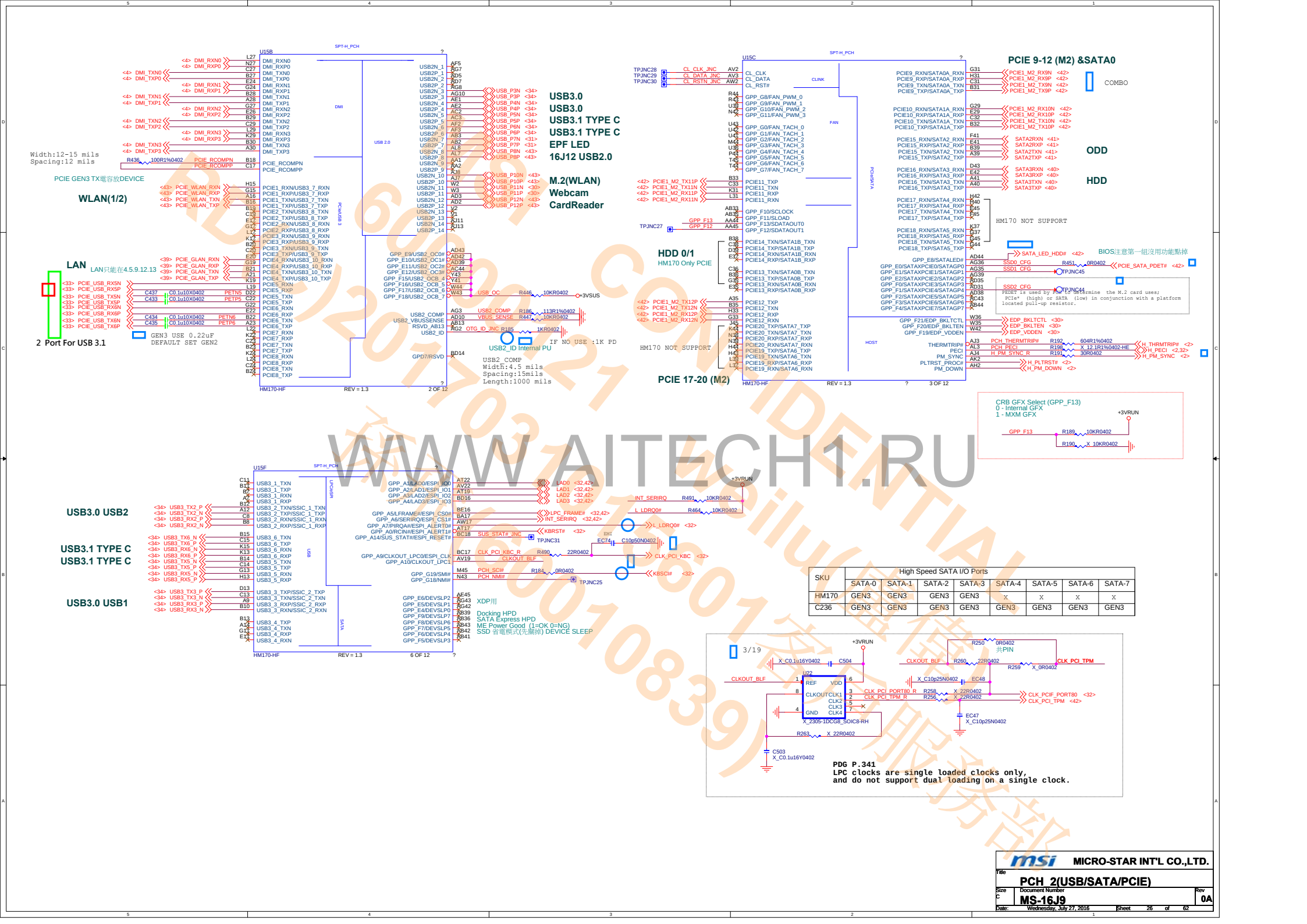
Date: Wednesday, July 27, 2016 Sheet 25 of 62



SMBALERT#
0 - Disable (Default Internal 20K PD)
1- Enable (AMT/SBA)

SML0ALERT#
0 - LPC (Default Internal 20K PD)
1- eSPI

PCH EDS Page 52

U15D — SPT-H_PCH — HM170-HF — REV = 1.3 — 4 OF 12

HDA_BITCLK, HDA_RST#, HDA_SDI0, HDA_SDI1, HDA_SDO, HDA_SYNC, RSVD_BD1, RSVD_BE2, DISPA_SDO, DISPA_SDI, DISPA_BCLK, GPP_D8/I2S0_SCLK, GPP_D7/I2S0_RXD, GPP_D6/I2S0_TXD, GPP_D5/I2S0_SFRM, GPP_D20/DMIC_DATA0, GPP_D19/DMIC_CLK0, GPP_D18/DMIC_DATA1, GPP_D17/DMIC_CLK1, RTCRST#, SRTCRST#, PCH_PWROK, RSMRST#, DSW_PWROK, GPP_C2/SMBALERT#, GPP_C0/SMBCLK, GPP_C1/SMBDATA, GPP_C5/SML0ALERT#, GPP_C3/SML0CLK, GPP_C4/SML0DATA, GPP_B23/SML1ALERT#/PCHHOT#, GPP_C6/SML1CLK, GPP_C7/SML1DATA

GPP_A12/BMBUSY#/ISH_GP6/SX_EXIT_HOLDOFF#, GPP_A8/CLKRUN#, GPD11/LANPHYPC, GPD9/SLP_WLAN#, DRAM_RESET#, GPP_B2/VRALERT#, GPP_B1, GPP_B0, GPP_G17/ADR_COMPLETE, GPP_B11, SYS_PWROK, WAKE#, GPD6/SLP_A#, SLP_LAN#, GPP_B12/SLP_S0#, GPD4/SLP_S3#, GPD5/SLP_S4#, GPD10/SLP_S5#, GPD8/SUSCLK, GPD0/BATLOW#, GPP_A15/SUSACK#, GPP_A13/SUSWARN#/SUSPWRDNACK, GPD2/LAN_WAKE#, GPD1/ACPRESENT, SLP_SUS#, GPD3/PWRBTN#, SYS_RESET#, GPP_B14/SPKR, PROCPWRGD, ITP_PMODE, JTAGX, JTAG_TMS, JTAG_TDO, JTAG_TDI, JTAG_TCK

要查一下
新的DDR由PCH做RESET
GPU_EVENT# <22>
GPP_B11 (GPO)
PCIE_WAKE# <33,39,43>
PM_SLP_S3# <32,53>
PM_SLP_S4# <32,46>
WLAN_SUSCLK <43>
SUSCLK <32>
SUSPWRACK <32>
AC_PRESENT <32>
PM_PWRBTN# <32>
PCH_JTAGX <2>
PCH_JTAG_TMS <2>
PCH_JTAG_TDO <2>
PCH_JTAG_TDI <2>
PCH_JTAG_TCK

+3VRUN
PM_SYSRST# R223 10KR0402
SMB_CLK_DIMM R458 1KR0402
SMB_DATA_DIMM R459 1KR0402

新的UMA HDMI/DP用
AUDIO_CPU_SDO_R, AUDIO_CPU_SDI, AUDIO_CPU_CLK_R
R206 30R0402 AUDIO_CPU_SDO
R207 30R0402 AUDIO_CPU_CLK

+3VSUS
R479 X_2.2KR0402 SMBALERT#
R484 X_20KR0402-2
R472 X_2.2KR0402 SML0ALERT#
150K for DCI enable
R455 X_150KR0402 SML1ALERT#
R466 1KR0402 SUS_SMBCLK
R474 1KR0402 SUS_SMBDATA
RN4 SML0_CLK, SML0_DATA, SML1_DATA, SML1_CLK
8P4R-1KR0402
RN9 LAN_WAKE#, BATLOW#, PCIE_WAKE#, AC_PRESENT
8P4R-10KR0402

JNC19 X_0402
RSMRST# JNC
SMBALERT#
SUS_SMBCLK
SUS_SMBDATA
SML0ALERT#
SML0_CLK
SML0_DATA
SML1ALERT#
SML1_CLK
SML1_DATA

TPJNC50 R489 0R0402
TPJNC51
TPJNC47 R465 X_0R0402
TPJNC48
TPJNC32
R463 100KR0402
Add R715 pull high +3VSUS
0 - Enable TCO
R251 X_1KR0402 +3VRUN
H_PWRGD <2>
HDA_SPKR

NN-DMN65D8LDW-7_SOT363-6-HF
Q28
SUS_SMBCLK D1 S1 G1 SMB_CLK_DIMM <8,9,43>
SUS_SMBDATA D2 S2 G2 SMB_DATA_DIMM <8,9,43>
連EC
連EC

+3VSUS R500 100KR0402
+5VRUN R488 2.2KR0402
PWOK_SMB
C792 C0.1u6.3X50402-HF
Q34 NN-DMN65D8LDW-7_SOT363-6-HF
檢討漏電流
PM_PCH_PWROK
PCH_PWROK

+3VALW
R537 1.5KR0402
R528 X_45.3KR1%0402
R543 X_0R0402
D13 1SS355_SOD323
D12 S-BAT54C_SOT23
選料注意切入電壓
RTCVCC
R548 20KR0402-2 RTCRST#
R545 20KR0402-2 SRTCRST#
C825 C1u10X0603
C831 C1u10X0603
C830 C1u10X0603
G2
RTC_P2
RTC_P3
R532 1KR0402
WIDTH:10MIL
BAT1
SD_53261_0210_2P
N32-10200Q0-A81

R492 0R0402
N-2N7002CK_SOT23-3-RH
Q36
RTC_CTL# <32>
R517 100KR0402
R551 X_0R0402

SKL PCH-H VCCRTC : does not exceed 3.2V
#543611 DG Figure 28-3. External Circuitry for RTC - Option 2a (Coin Battery)

60階
BCR1220H2.8AM1ZB
BAT2
D06-0105701-K26

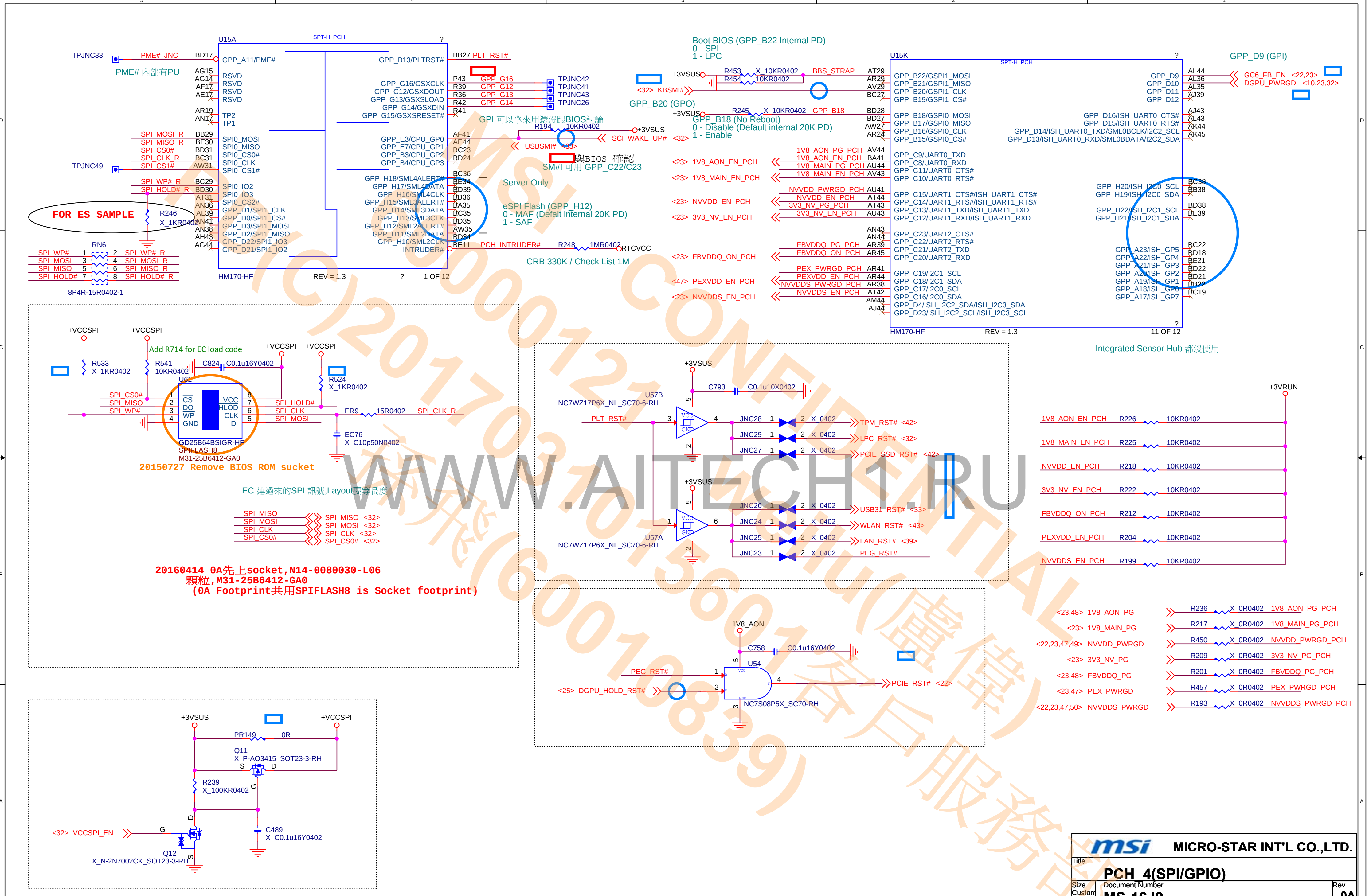
<37> CODEC_HDA_BIT_CLK
<37> CODEC_HDA_SDOUT
<37> CODEC_HDA_RST#
<37> CODEC_HDA_SYNC
RN5 HDA_BITCLK, HDA_SDO, HDA_RST#, HDA_SYNC
8P4R-33R0402
EC42 X_C10p50N0402
EC43 X_C10p50N0402
EC44 X_C10p50N0402
EC45 X_C10p50N0402

待改
+3VSUS
C471 C0.1u6.3X50402-HF
PCH_PWROK
<32> EC_PCH_PWROK
EC delay 100ms
SYS_PWROK
U18 NC7S08P5X_SC70-RH

+3VSUS
C525 C0.1u6.3X50402-HF
C487 C0.1u6.3X50402-HF
<51> CPU_PWROK
<2,32,35,51> EC_ALLSYSPG
RUN最後一根
PCH_PWROK
U16 NC7S08P5X_SC70-RH

Title	PCH_3(HDA/RTC/SMBUS)
Size / Custom	Document Number: MS-16J9
Rev	0A
Date:	Wednesday, July 27, 2016
Sheet	27 of 62

MICRO-STAR INT'L CO.,LTD.

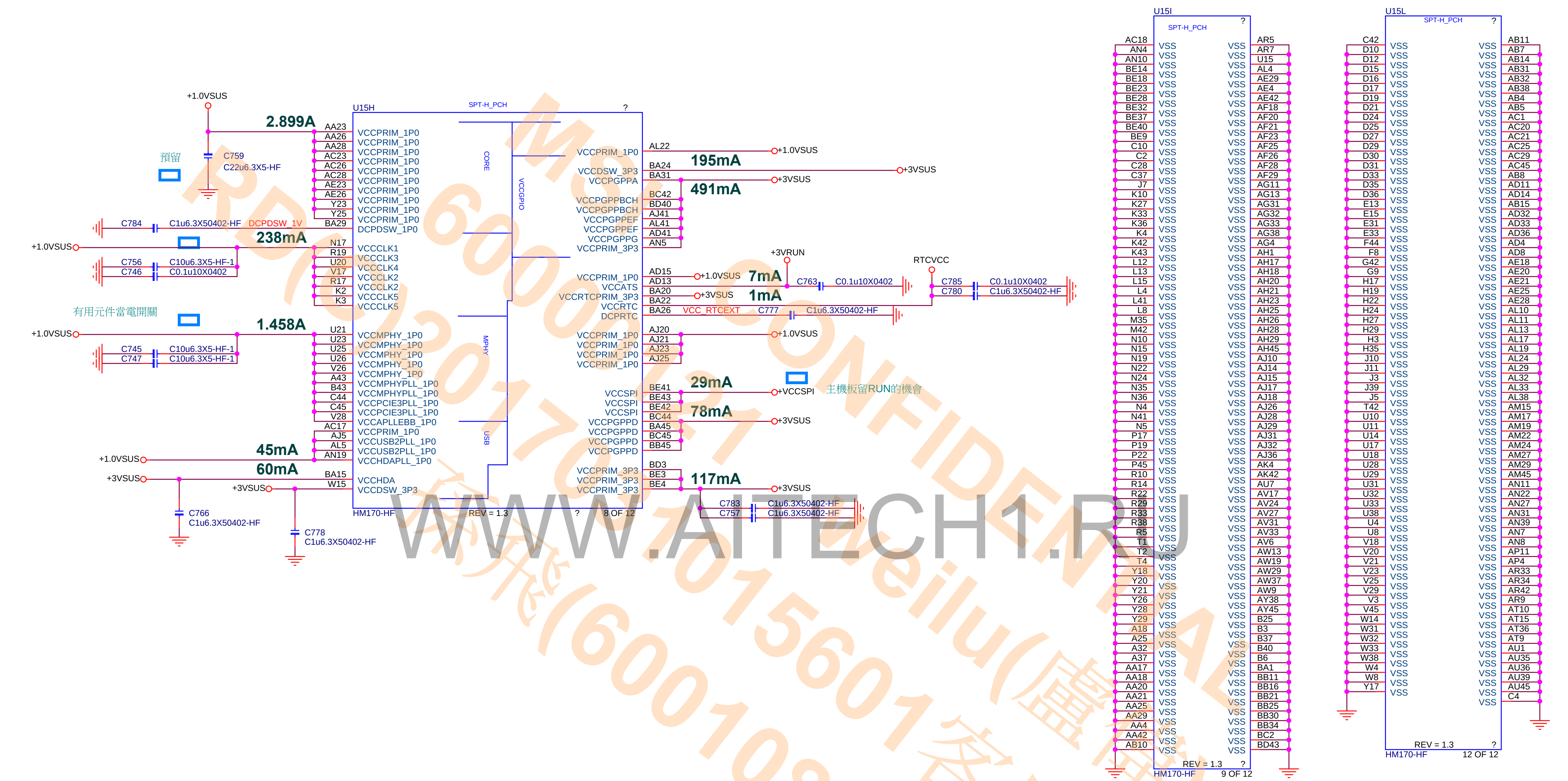


MICRO-STAR INT'L CO.,LTD.

Title: PCH_4(SPI/GPIO)

Size: Custom | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 28 of 62



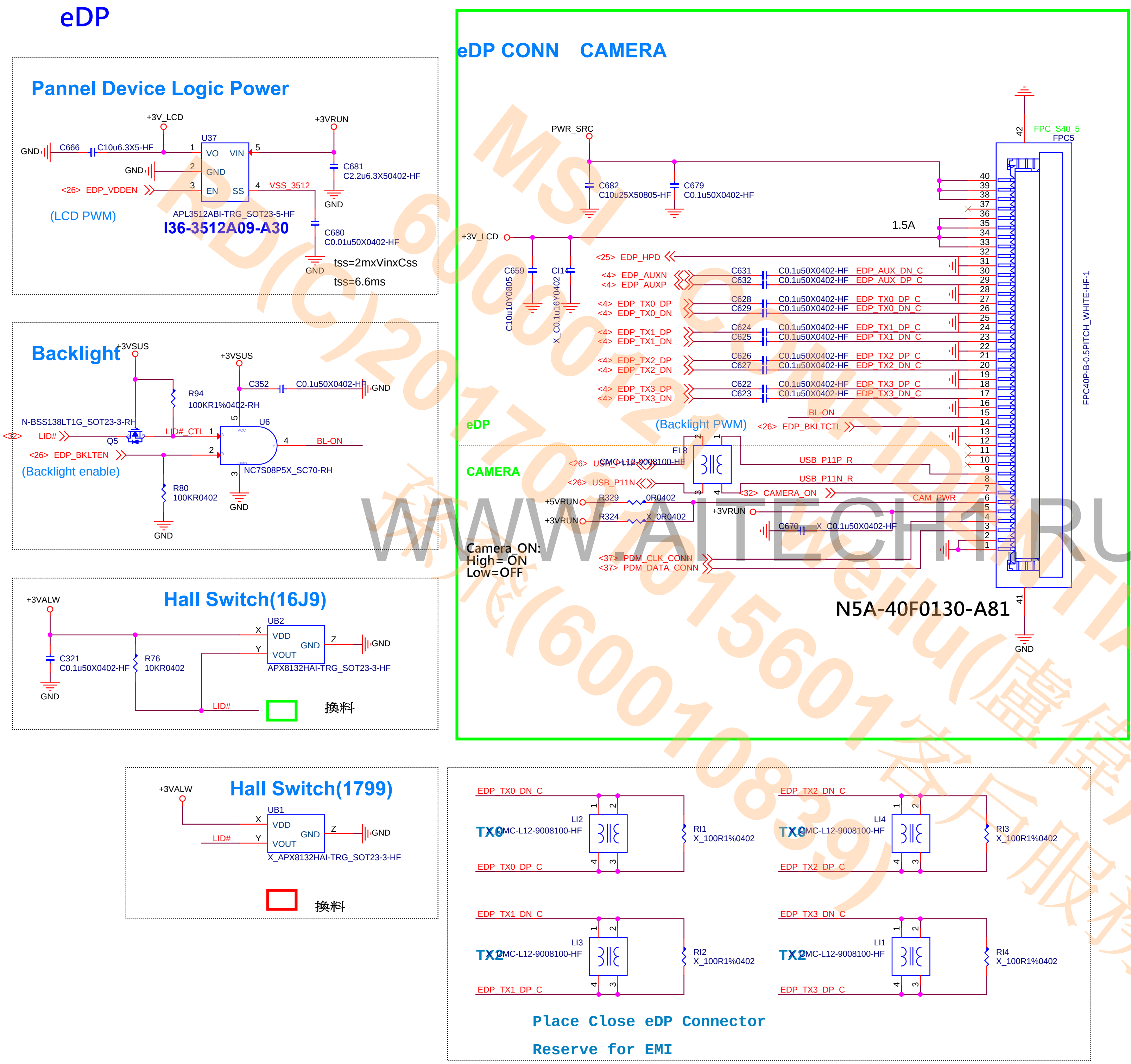
msi MICRO-STAR INT'L CO.,LTD.

Title: PCH_5(Power1)

Size: Custom | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 29 of 62

eDP



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

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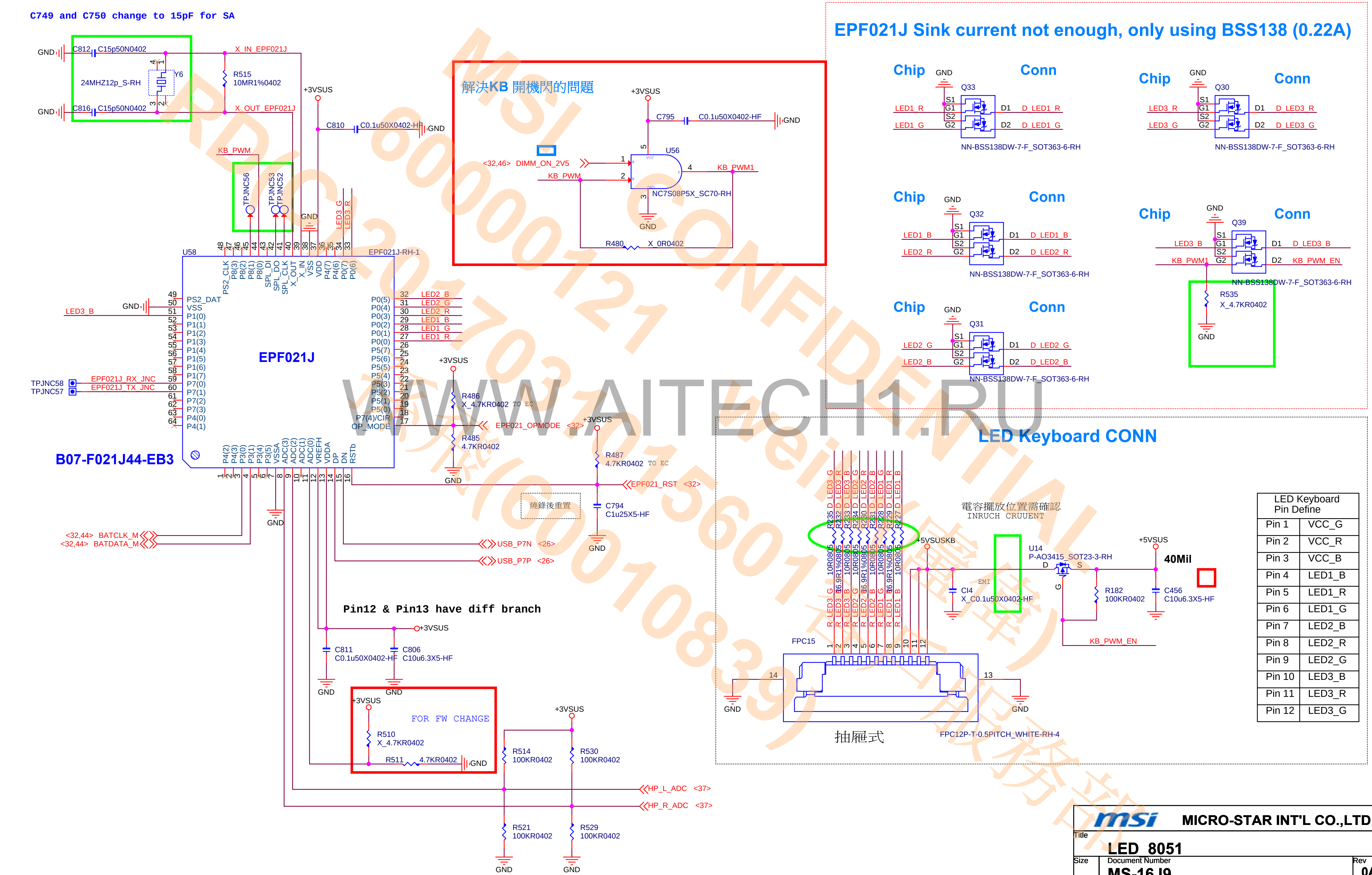
Title: eDP /Camera

Size | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 30 of 62

LED 8051 Controller



LED Keyboard Pin Define

Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

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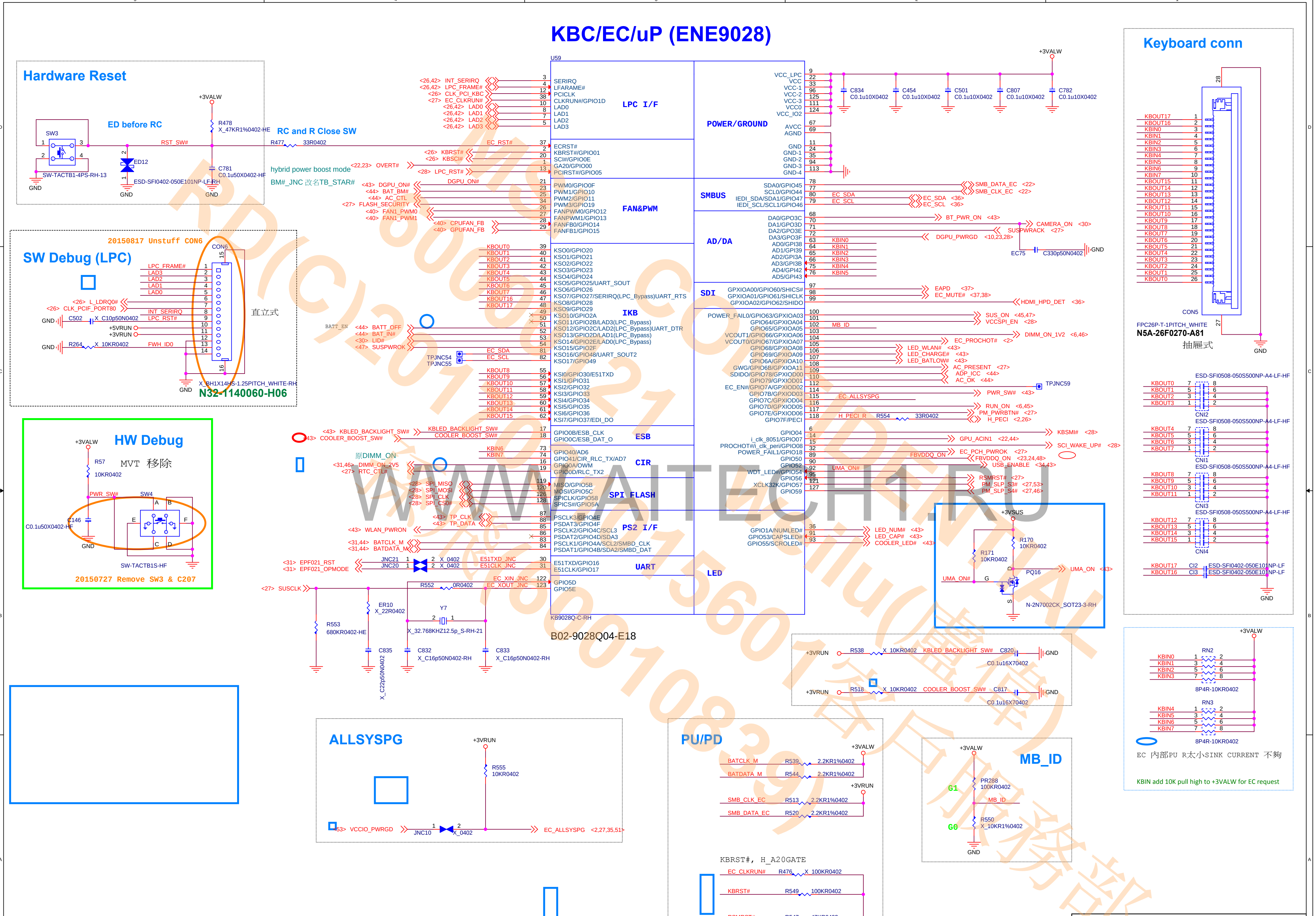
Title: LED_8051

Size | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 31 of 62



MICRO-STAR INT'L CO.,LTD.

Title: KBC(KB3930QFB1)

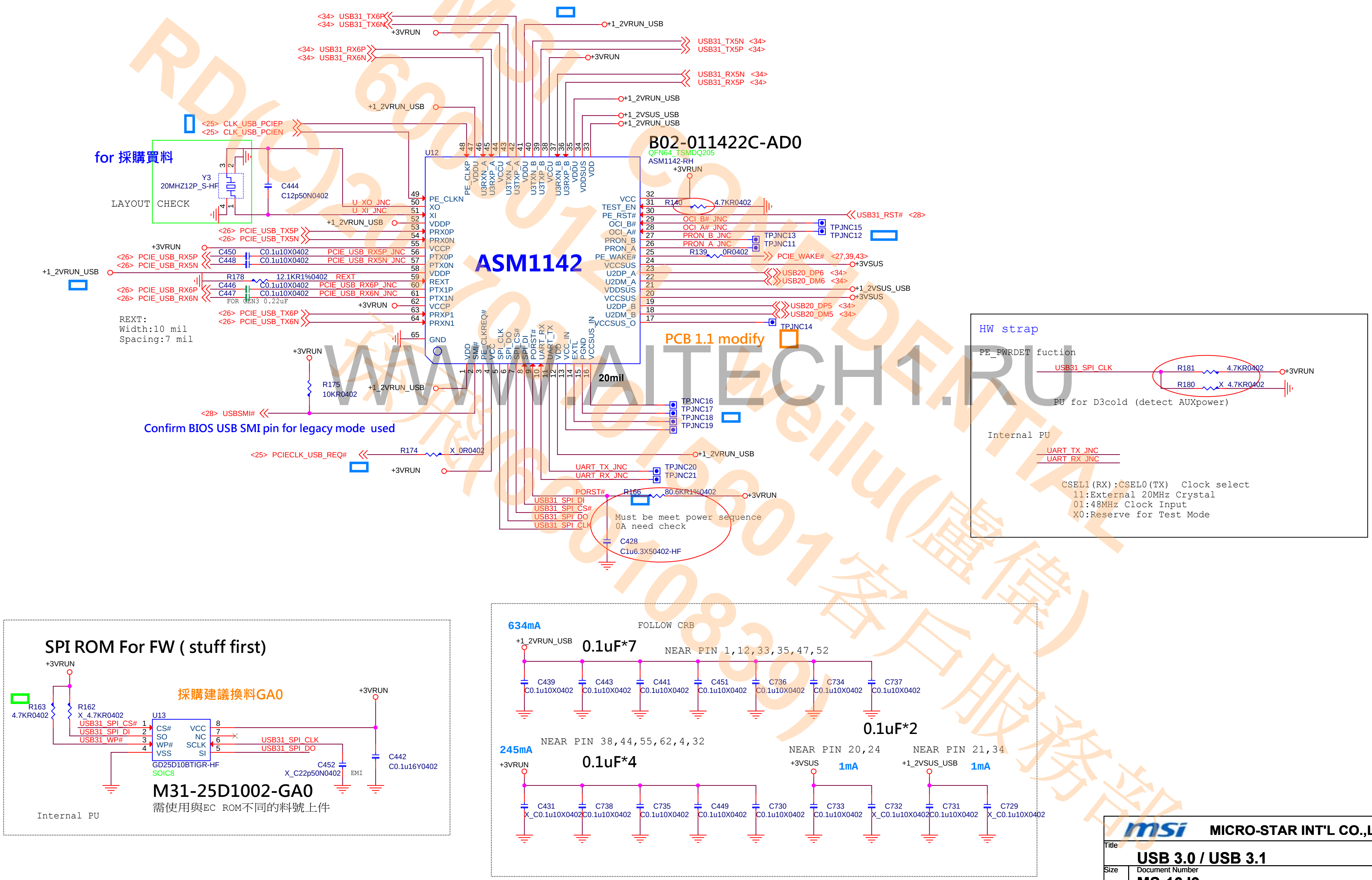
Document Number: MS-16J9

Rev: 0A

Date: Wednesday, July 27, 2016 — Sheet 32 of 62

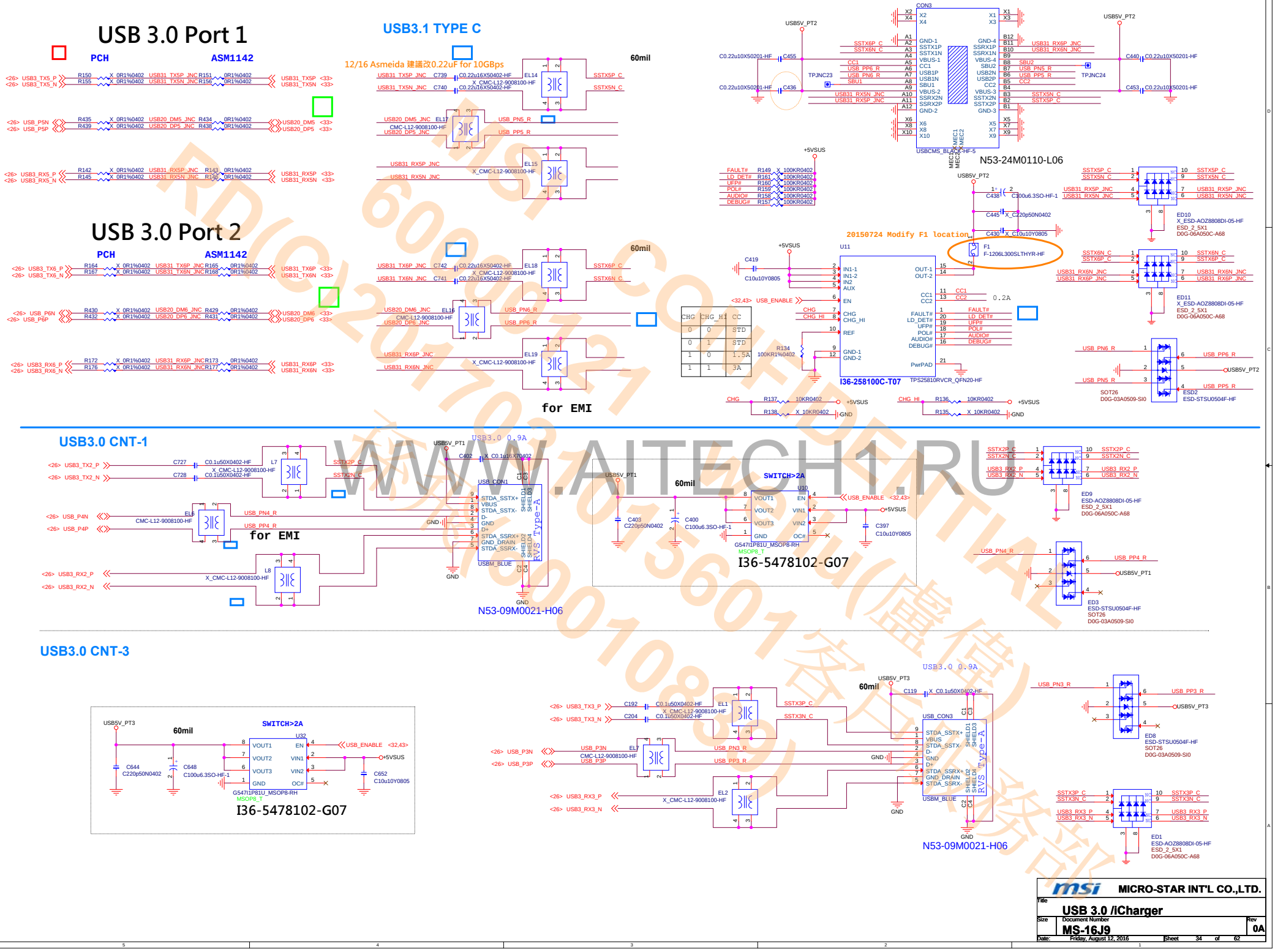
USB 3.0/ USB.3.1

PCIE to USB 3.1



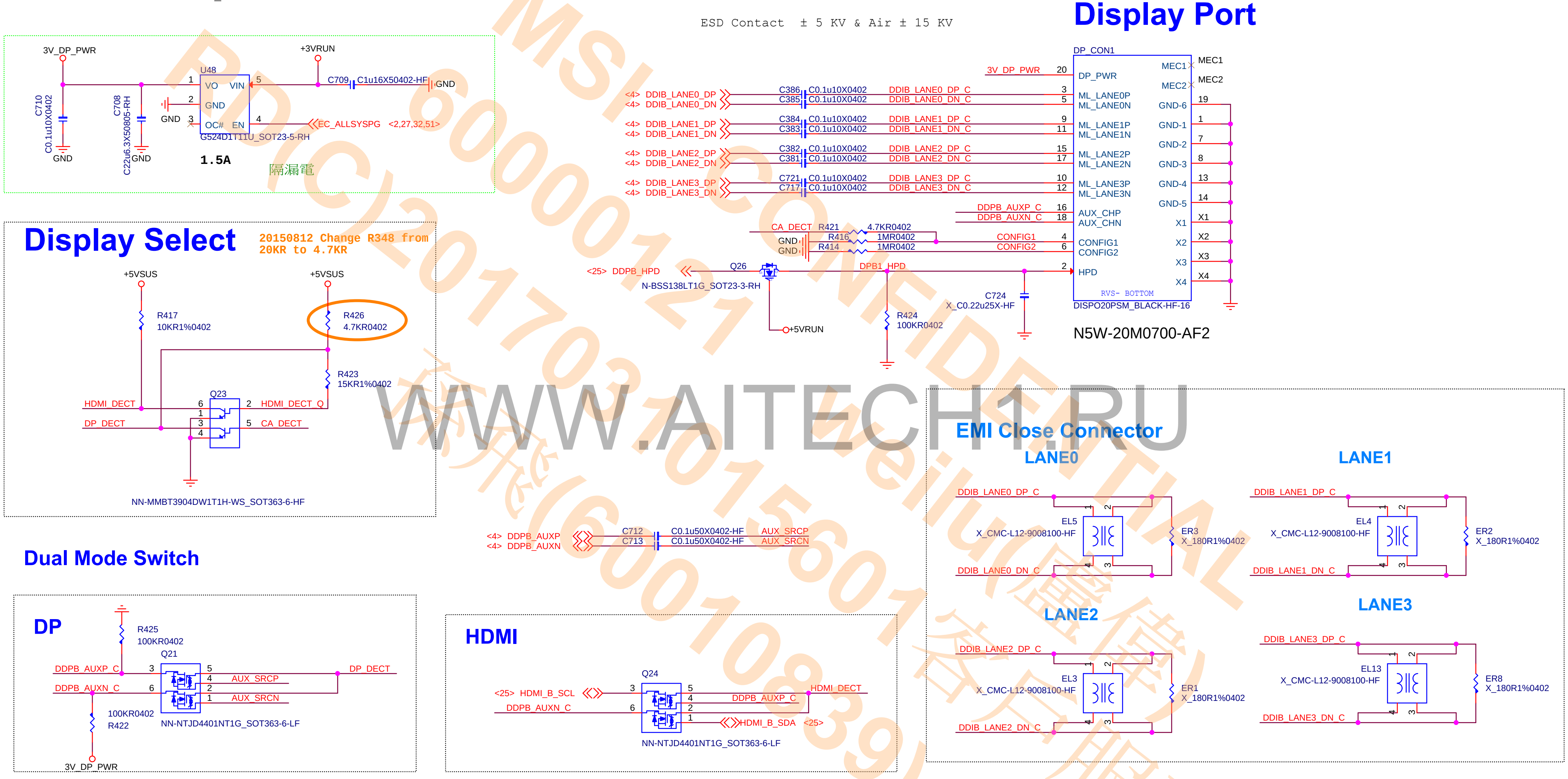
MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 / USB 3.1	
Size	Document Number: MS-16J9	Rev: 0A
Date: Wednesday, July 27, 2016	Sheet 33 of 62	



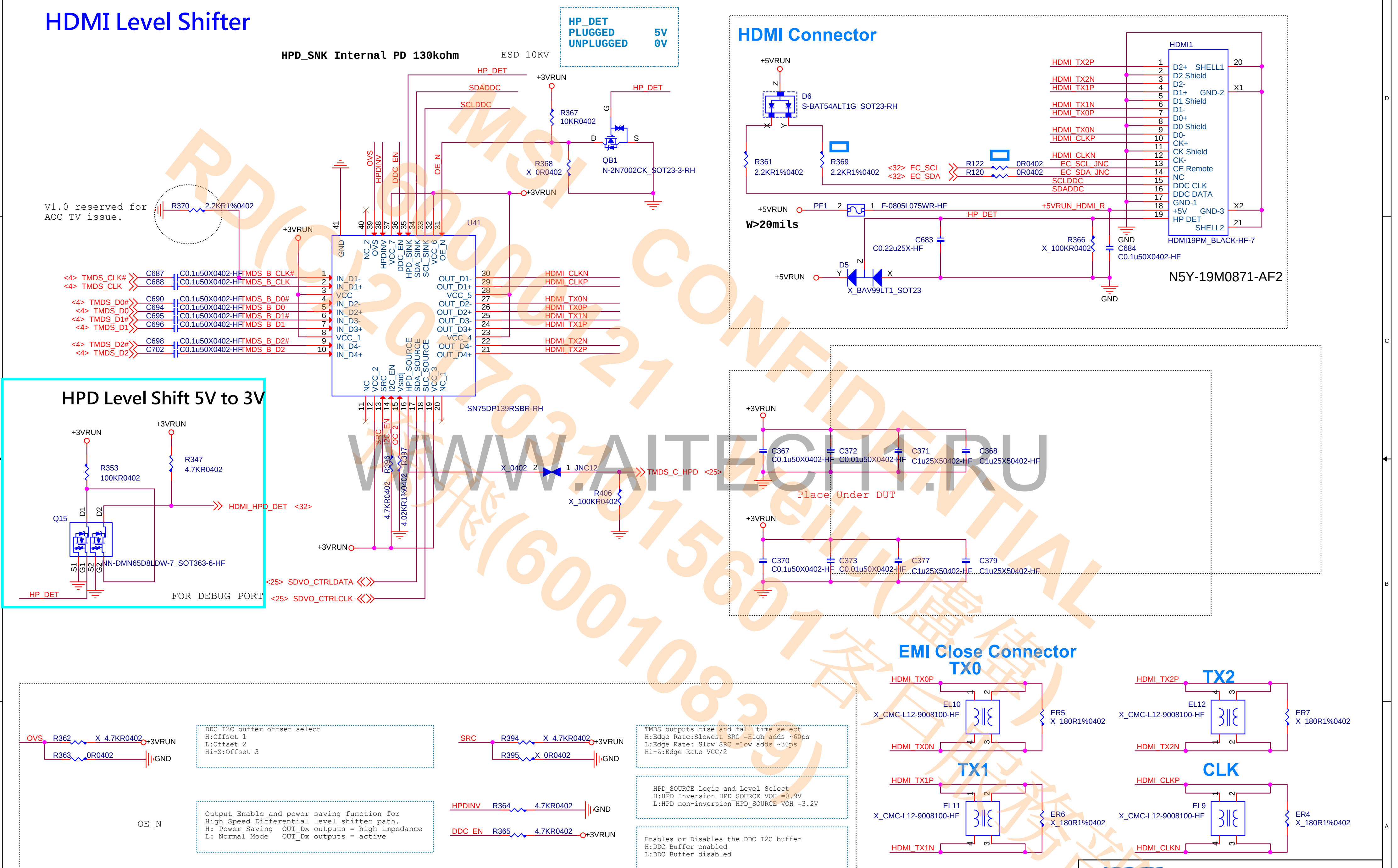
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



MSI MICRO-STAR INT'L CO.,LTD.

Title	DP	
Size	Document Number MS-16J9	Rev 0A
Date: Wednesday, July 27, 2016	Sheet 35 of 62	



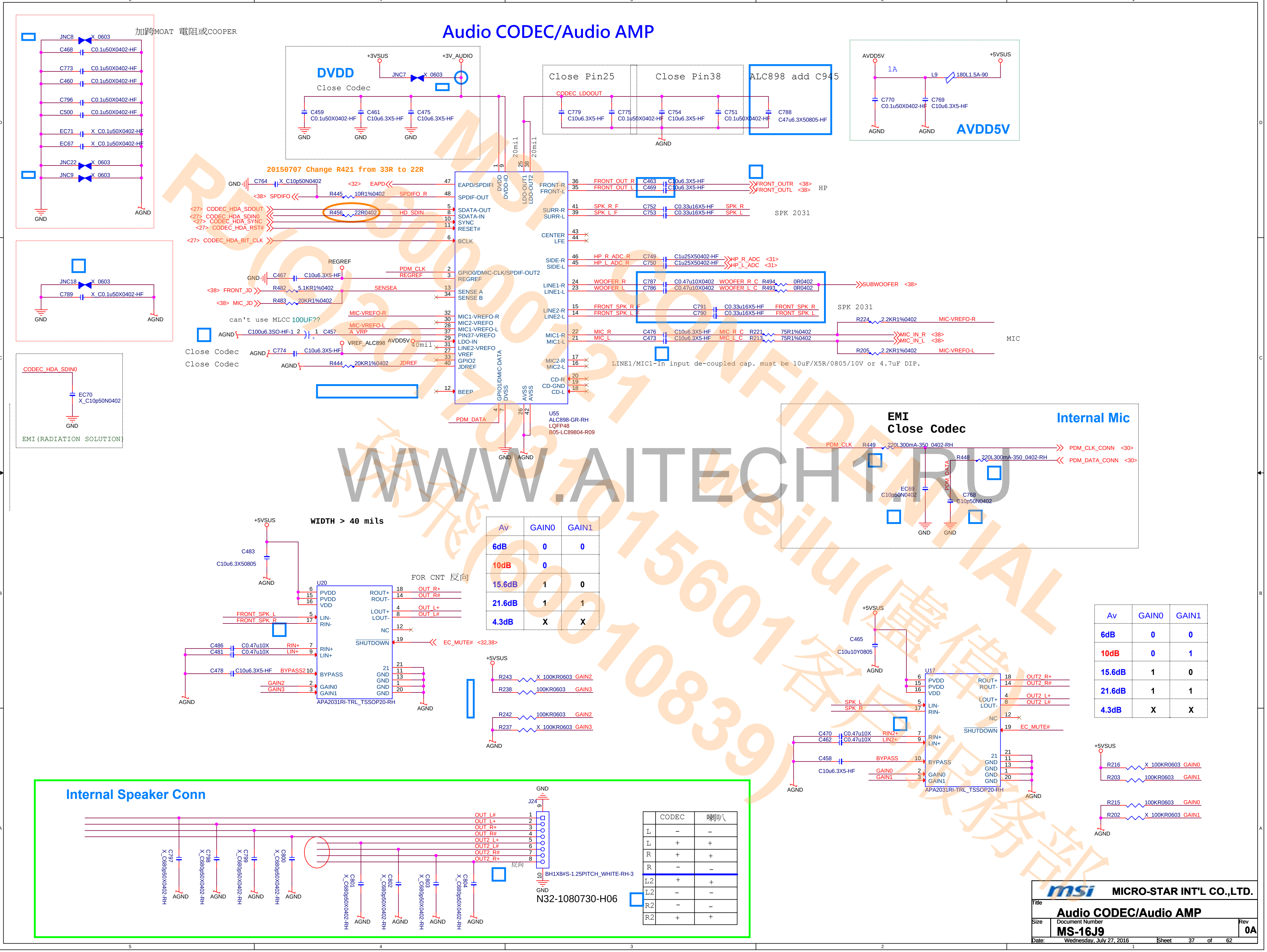
MICRO-STAR INT'L CO.,LTD.

Title: HDMI DP139

Size | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 36 of 62

Audio CODEC/Audio AMP



Av	GAIN0	GAIN1
6dB	0	0
10dB	0	
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

	CODEC	喇叭
L	–	–
L	+	+
R	+	+
R	–	–
L2	+	+
L2	–	–
R2	–	–
R2	+	+

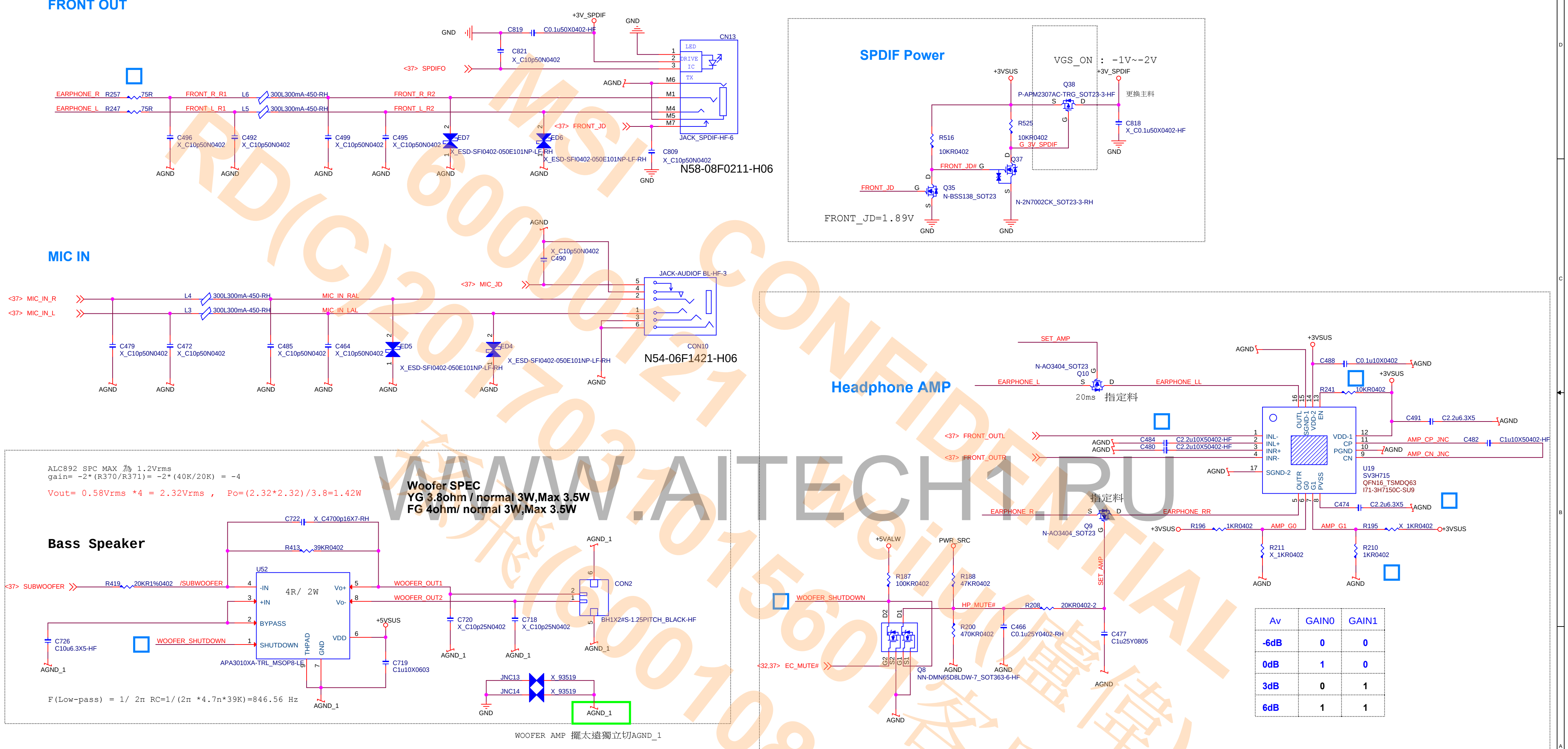
MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

Size | Document Number: MS-16J9 | Rev: 0A

Date: Wednesday, July 27, 2016 | Sheet 37 of 62

Audio CONN /Woffer



Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

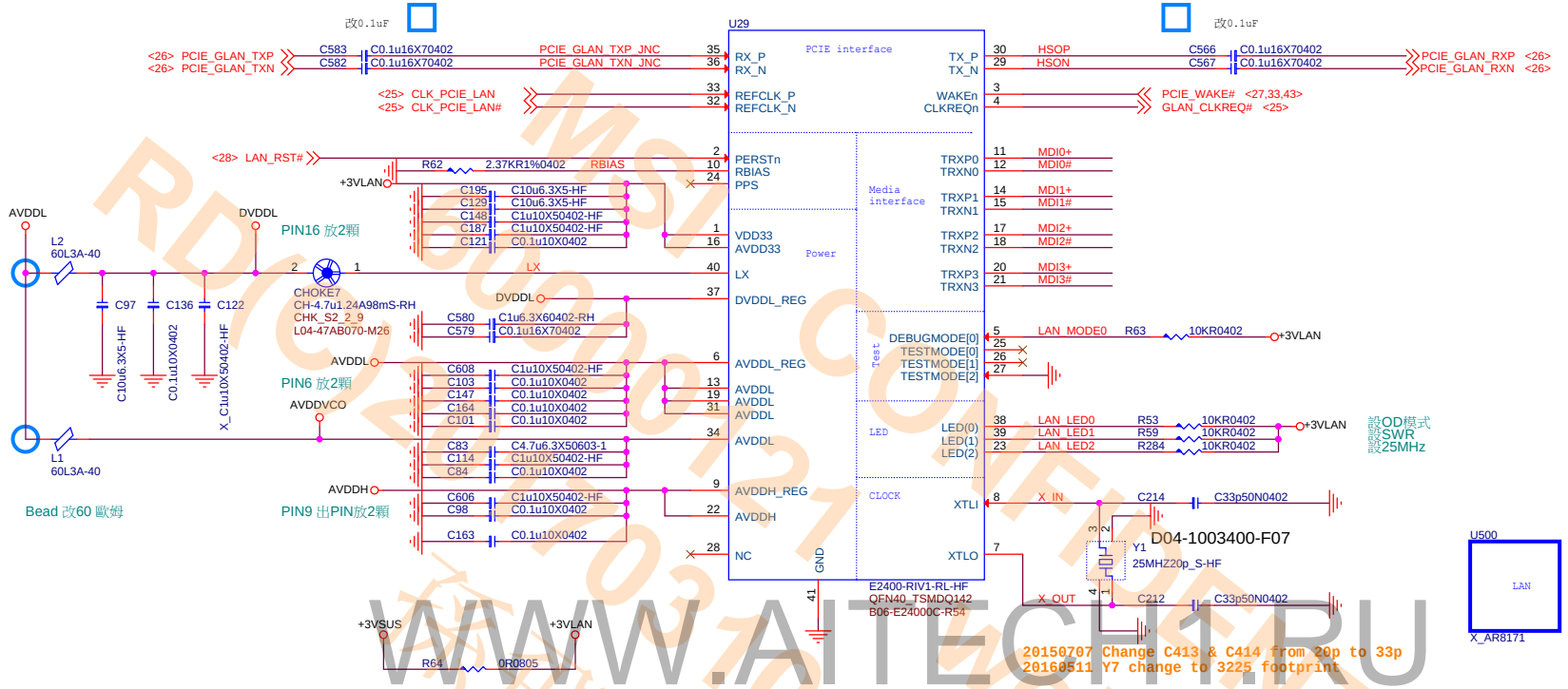
MICRO-STAR INT'L CO.,LTD.

Title: Audio / Woffer

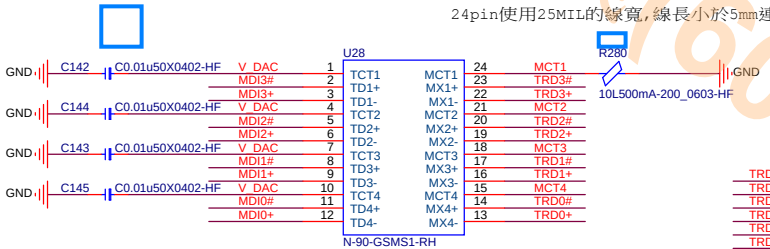
Size | Document Number: MS-16J9 | Rev: 0A

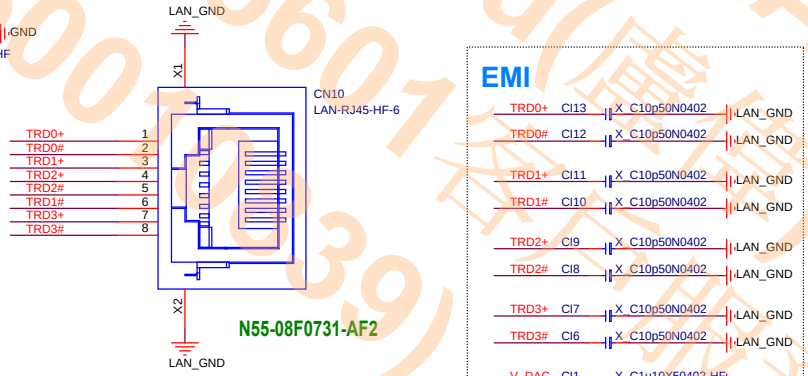
Date: Wednesday, July 27, 2016 | Sheet 38 of 62

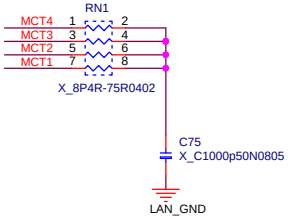
GIGA LAN(BigFoot BFN2400B)

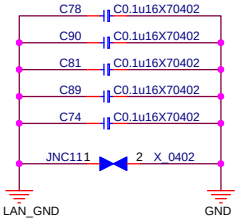


24pin使用25MIL的線寬,線長小於5mm連接GND

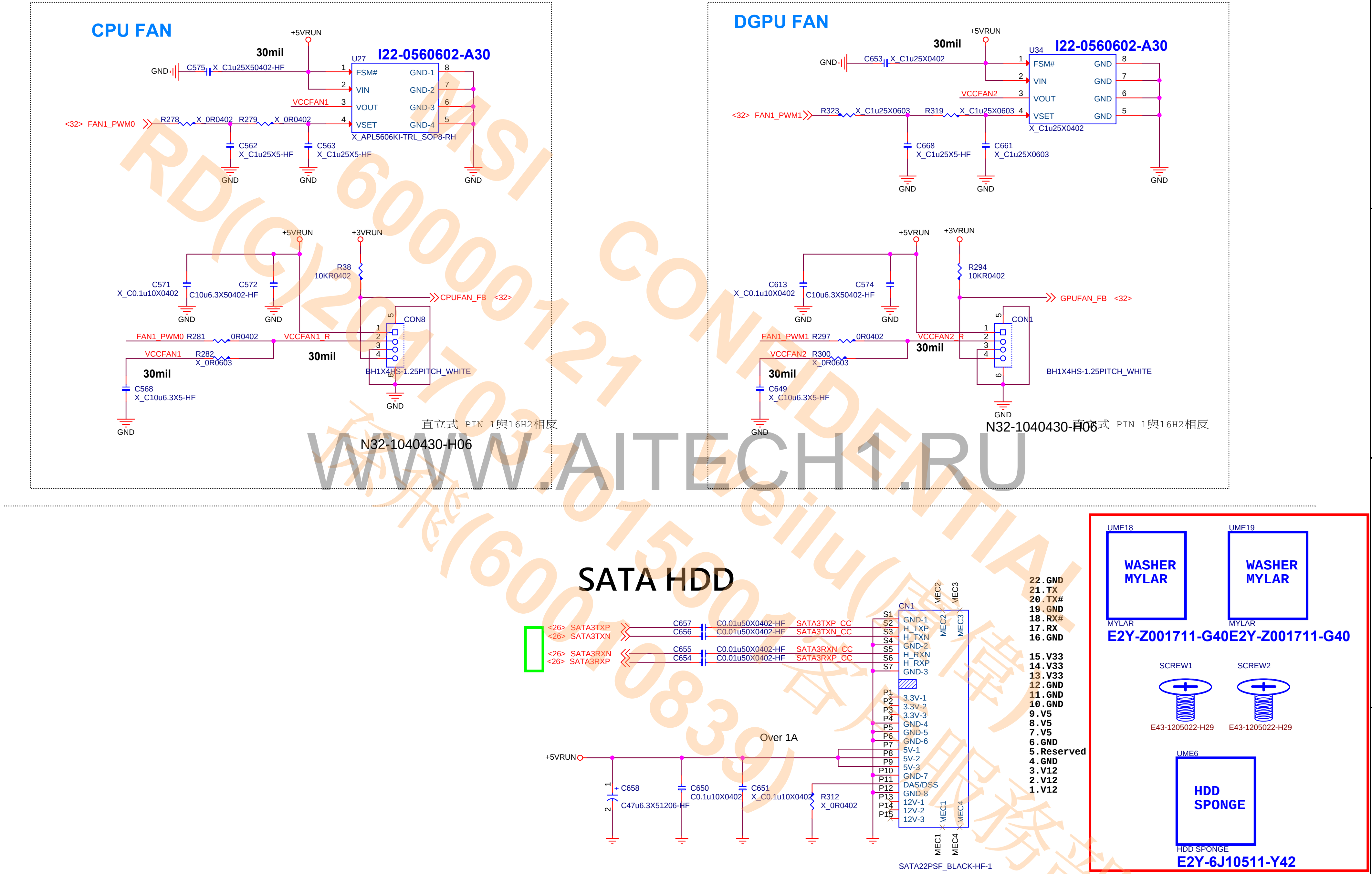








MSI	MICRO-STAR INT'L CO.,LTD.		
Title	GIGA LAN(BigFoot BFN2400/AR8171)		
Size	Document Number MS-16J9		Rev 0A
Date: Wednesday, July 27, 2016	Sheet 39 of 62		

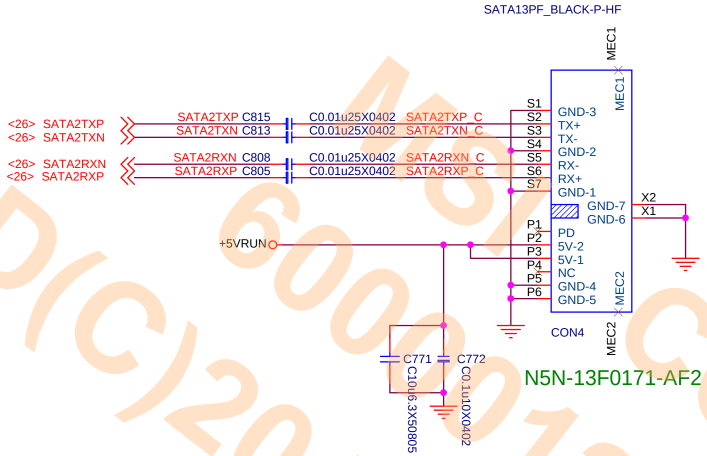


Title: ODD/HDD/FAN

Size	Document Number	Rev
A3	MS-16J9	0A

Date: Wednesday, July 27, 2016

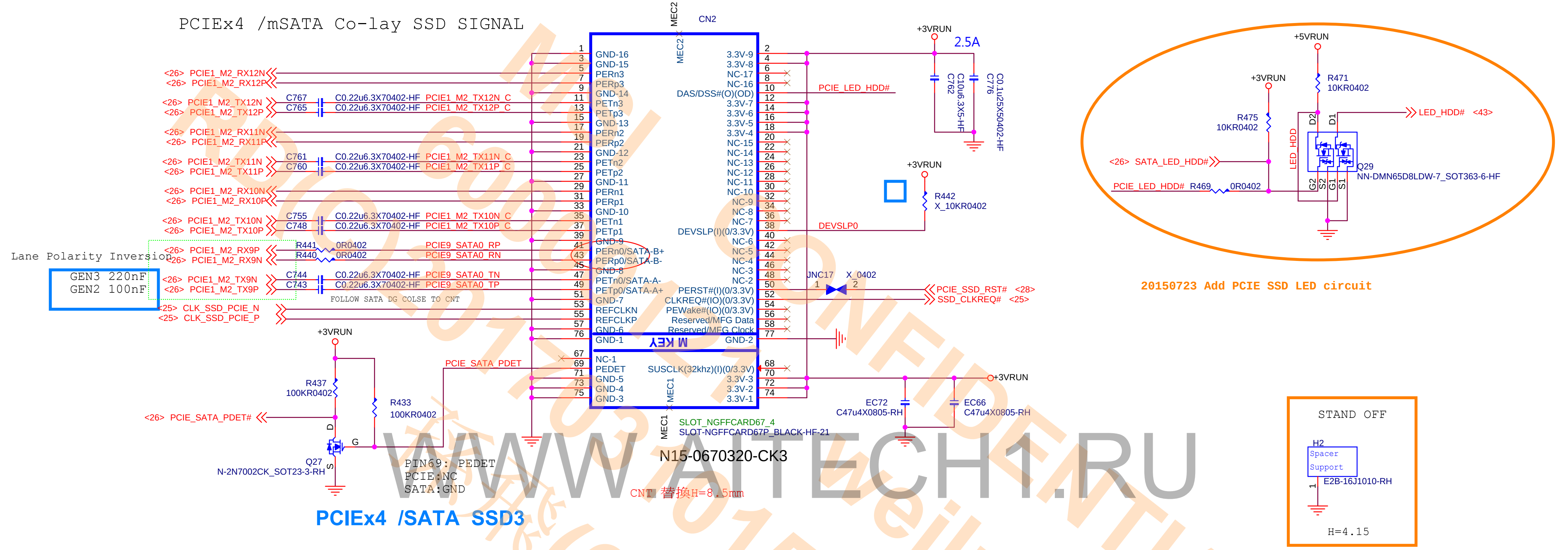
SATA ODD



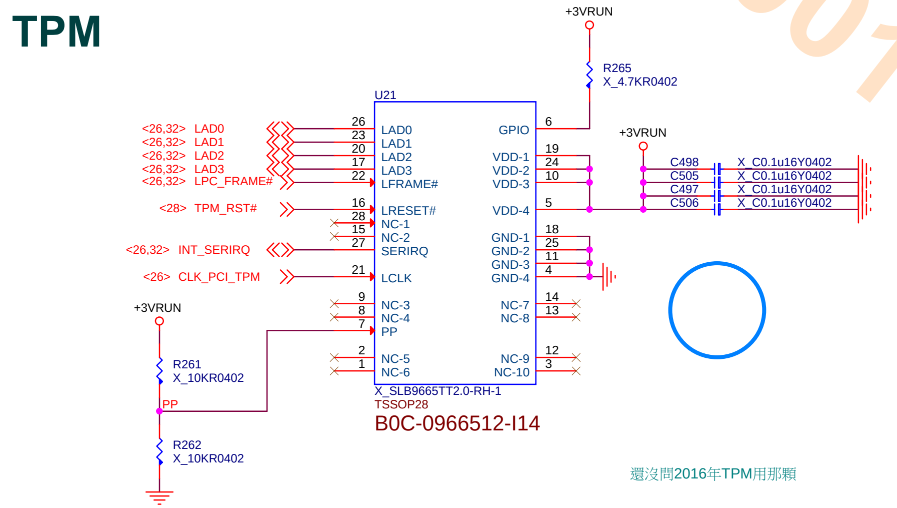
MICRO-STAR INT'L CO.,LTD.

Title	FBA_CMD18		
Size	Document Number: MS-16J9		Rev: 0A
Date:	Wednesday, July 27, 2016	Sheet 41 of 62	

PCIEx4 /mSATA Co-lay SSD SIGNAL



TPM

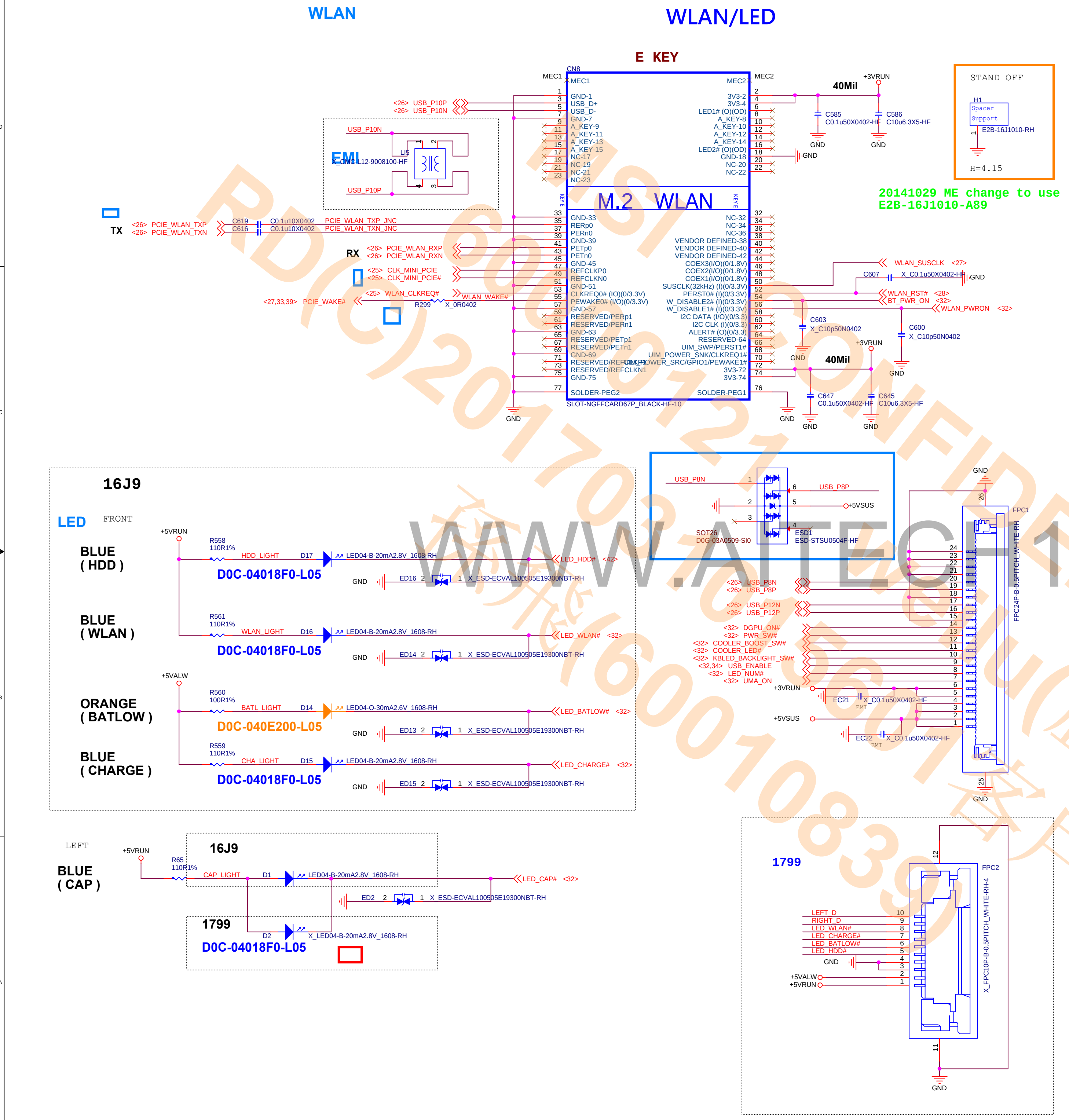


還沒問2016年TPM用那顆

MICRO-STAR INT'L CO.,LTD.

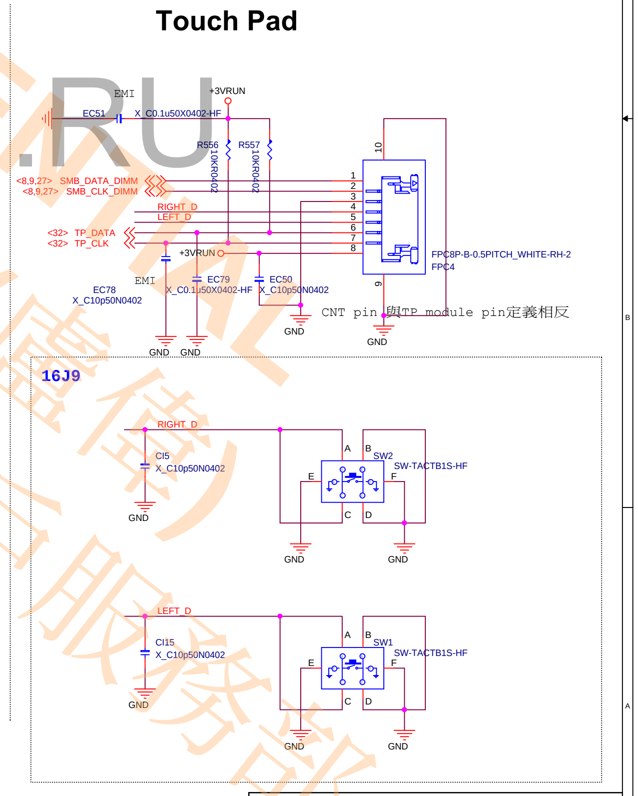
Title	SSD		
Size	Document Number: MS-16J9		Rev 0A
Date: Wednesday, July 27, 2016	Sheet 42 of 62		

WLAN/LED



Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V

Touch Pad



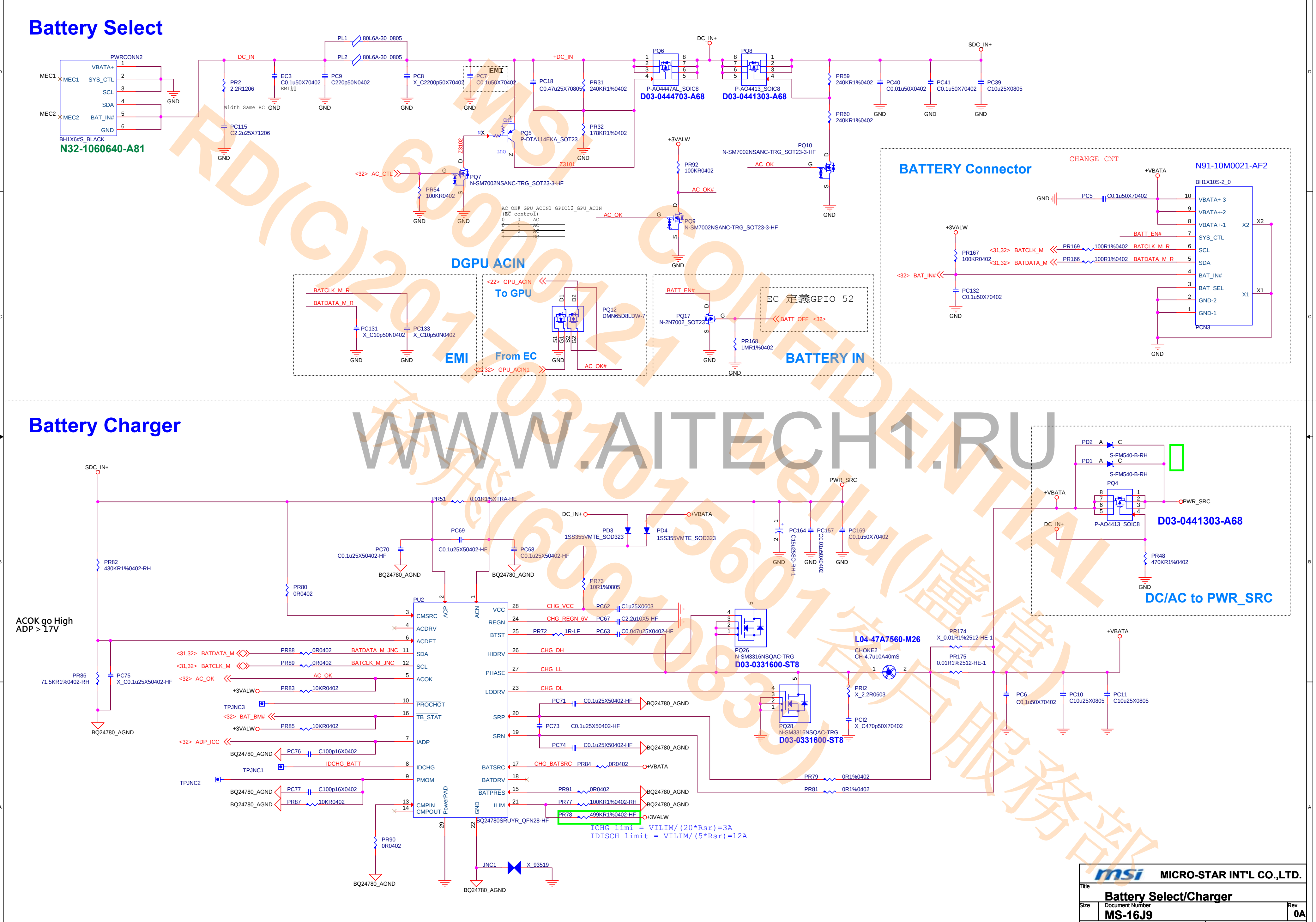
MICRO-STAR INT'L CO.,LTD.

Title: WLAN /LED/TP

Document Number: MS-16J9 — Rev 0A

Date: Friday, August 12, 2016 — Sheet 43 of 62

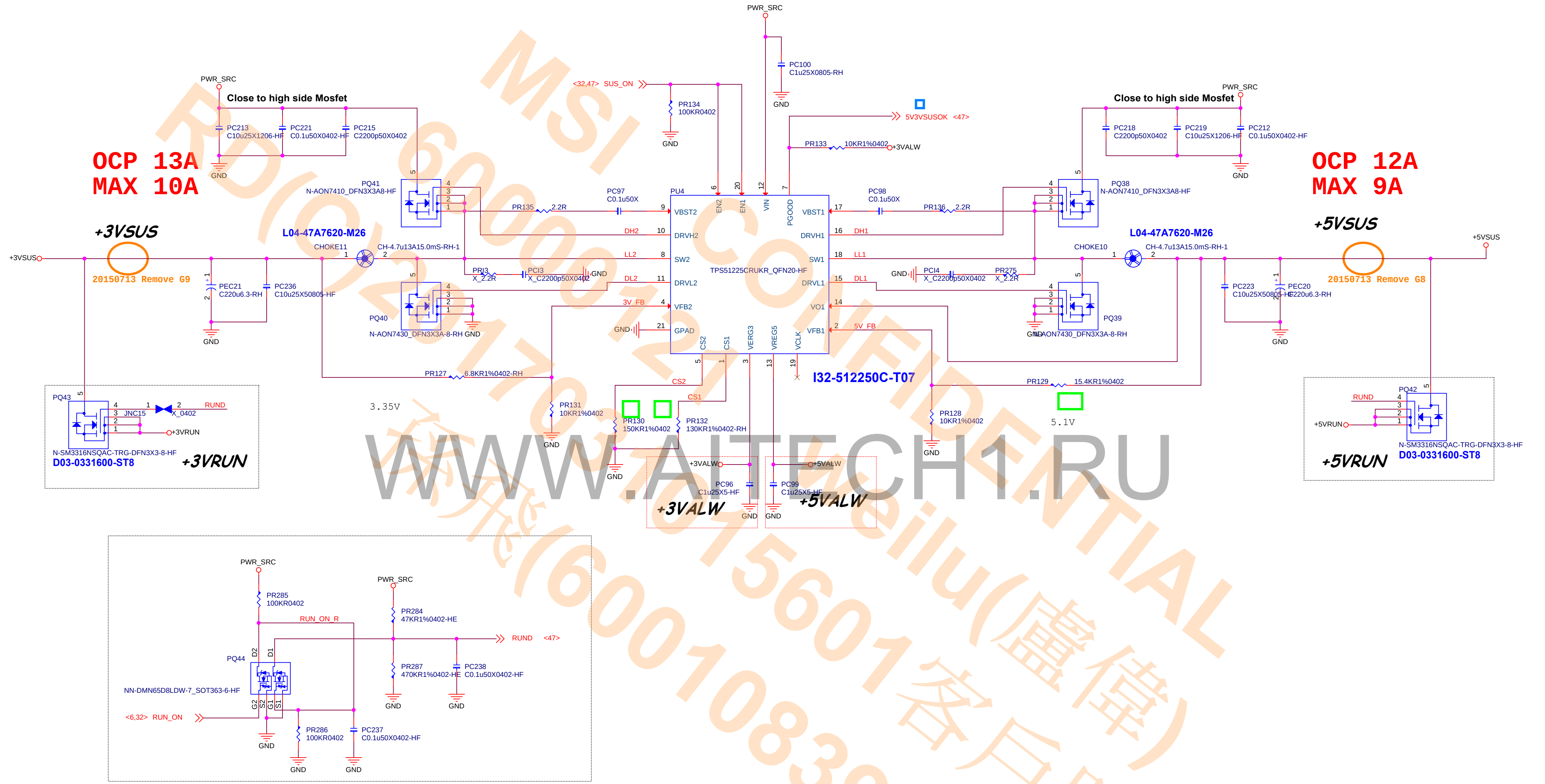
Battery Select/Charger



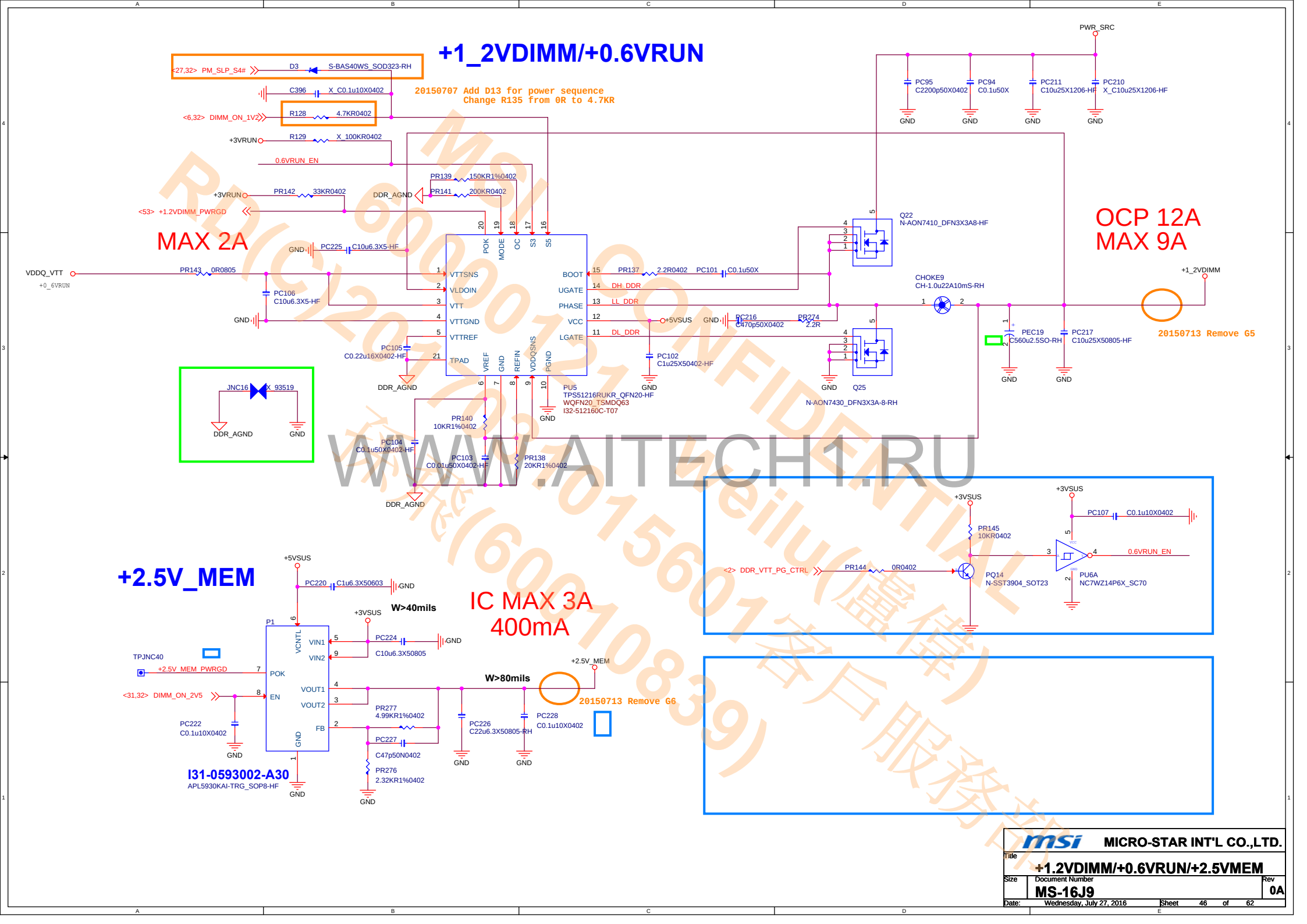
MICRO-STAR INT'L CO.,LTD.

Title	Battery Select/Charger	
Size	Document Number: MS-16J9	Rev: 0A
Date: Tuesday, September 06, 2016	Sheet 44 of 62	

System Power



msi	MICRO-STAR INT'L CO.,LTD.	
Title: System Power		
Size	Document Number: MS-16J9	Rev: 0A
Date: Wednesday, July 27, 2016	Sheet 45 of 62	


+1_2VDIMM/+0.6VRUN
20150707 Add D13 for power sequence
Change R135 from 0R to 4.7KR
MAX 2A
OCP 12A
MAX 9A
20150713 Remove G5
+2.5V_MEM
IC MAX 3A
400mA
W>40mils
W>80mils
20150713 Remove G6
I31-0593002-A30
APL5930KAI-TRG_SOP8-HF
TPS51216RUKR_QFN20-HF
WQFN20_TSMDQ63
I32-512160C-T07
N-AON7410_DFN3X3A8-HF
N-AON7430_DFN3X3A-8-RH
N-SST3904_SOT23
NC7WZ14P6X_SC70
CONFIDENTIAL
WWW.AITECH1.RU
MICRO-STAR INT'L CO.,LTD.
+1.2VDIMM/+0.6VRUN/+2.5VMEM
MS-16J9
0A
Wednesday, July 27, 2016
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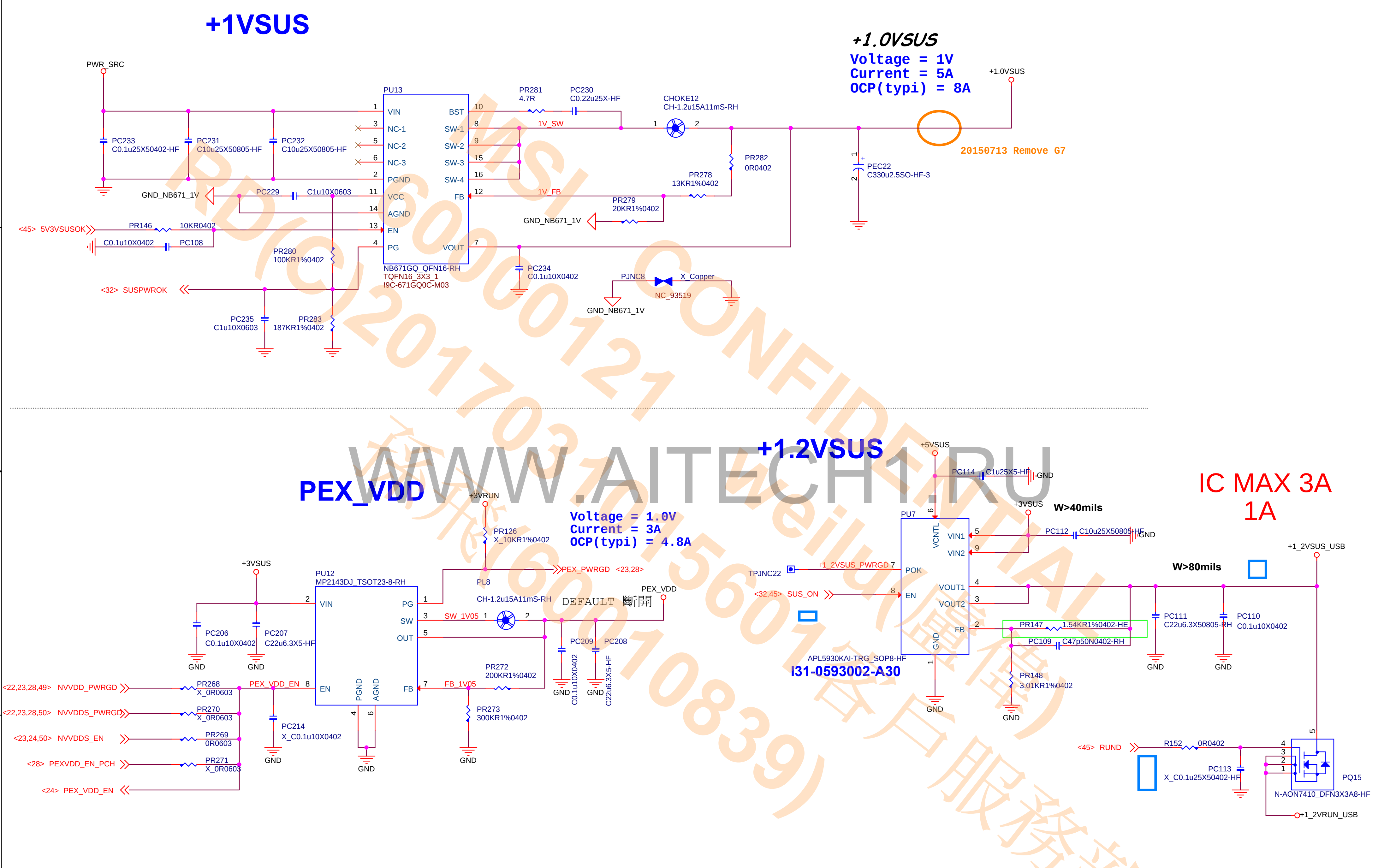

MICRO-STAR INT'L CO.,LTD.

Title: 1VSUS /PEX_VDD/1.2VSUS

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	MS-16J9	0A

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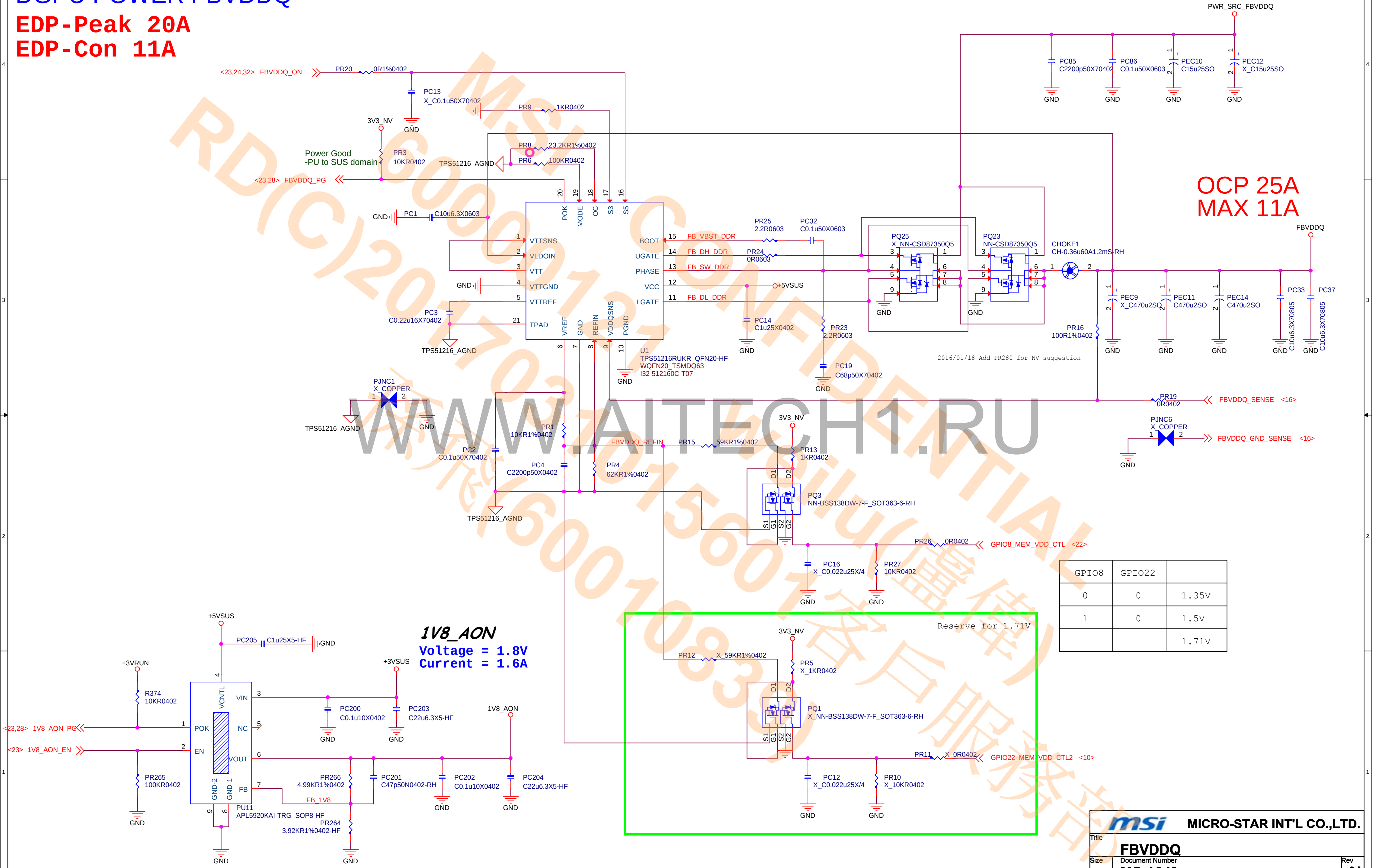
PAGE53: FBVDDQ

DGPU POWER FBVDDQ

EDP-Peak 20A
EDP-Con 11A



GPIO8	GPIO22	
0	0	1.35V
1	0	1.5V
		1.71V

MICRO-STAR INT'L CO.,LTD.

Title: FBVDDQ

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DGPU POWER / UP9509P

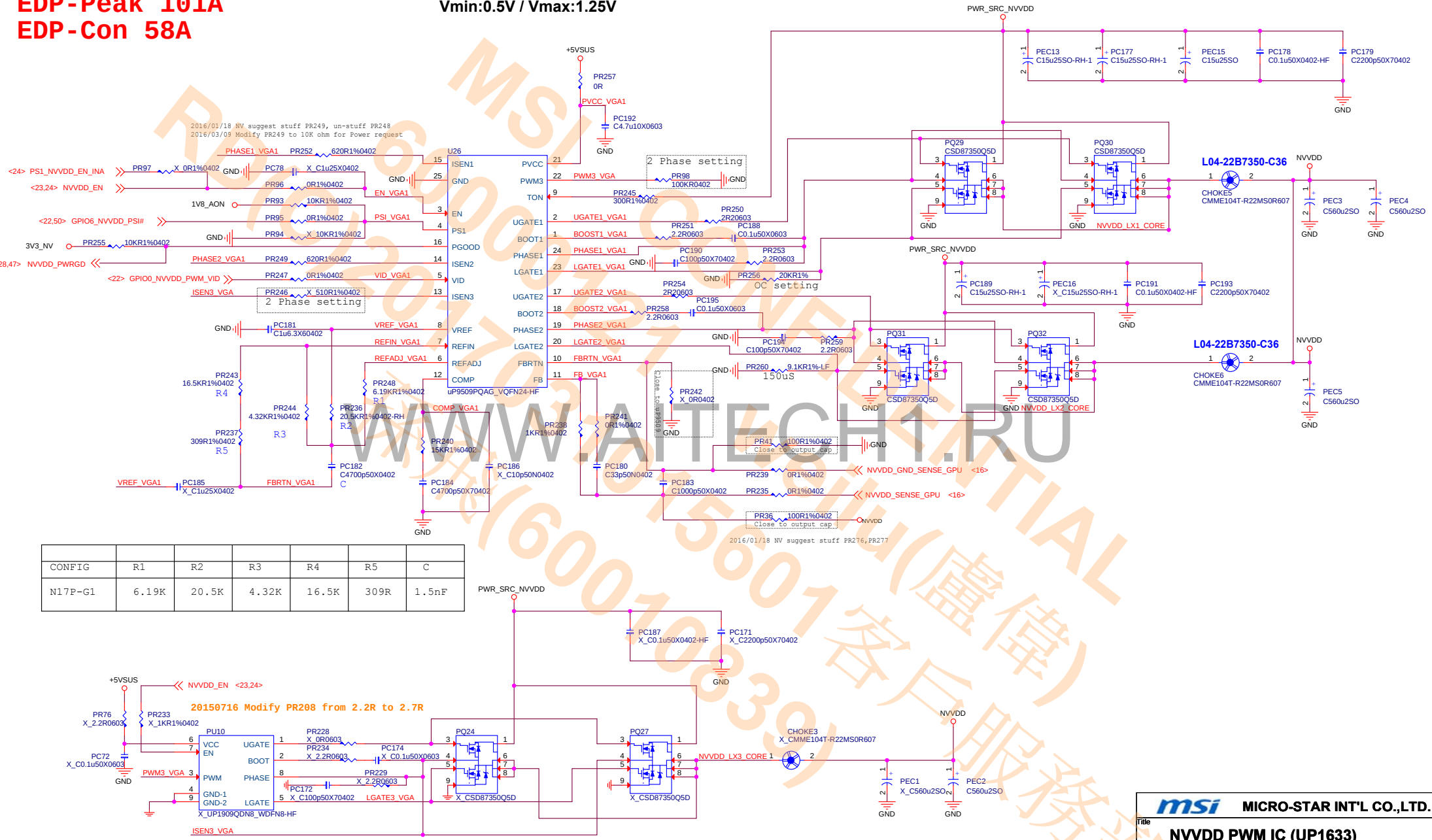
EDP-Peak 101A

EDP-Con 58A

DGPU POWER NVVDD

VBoot:0.8V

Vmin:0.5V / Vmax:1.25V



CONFIG	R1	R2	R3	R4	R5	C
N17P-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

Title	MICRO-STAR INT'L CO.,LTD.		
	NVVDD PWM IC (UP1633)		
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DGPU POWER / UP1666P

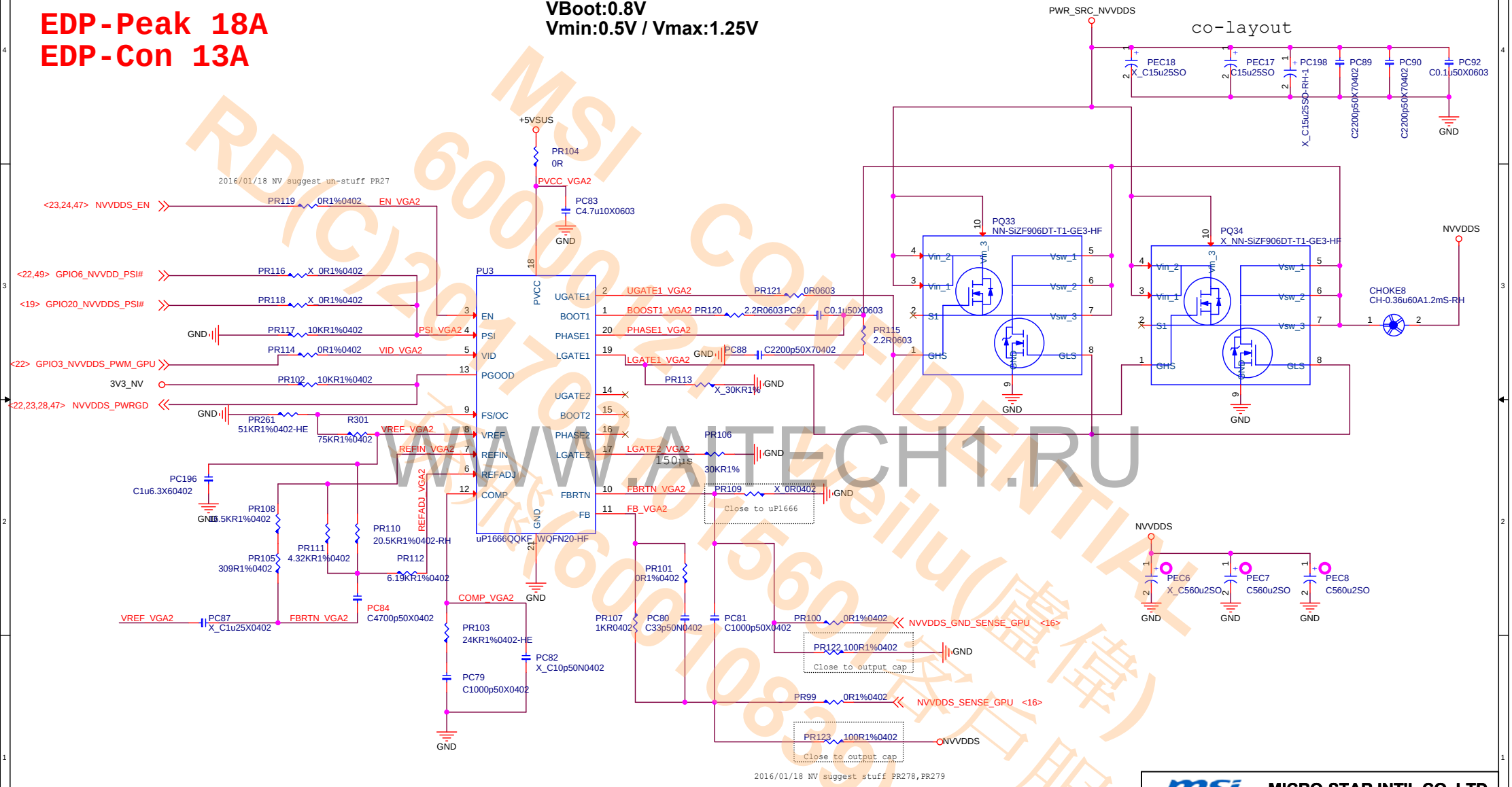
EDP-Peak 18A

EDP-Con 13A

DGPU POWER NVVDDS

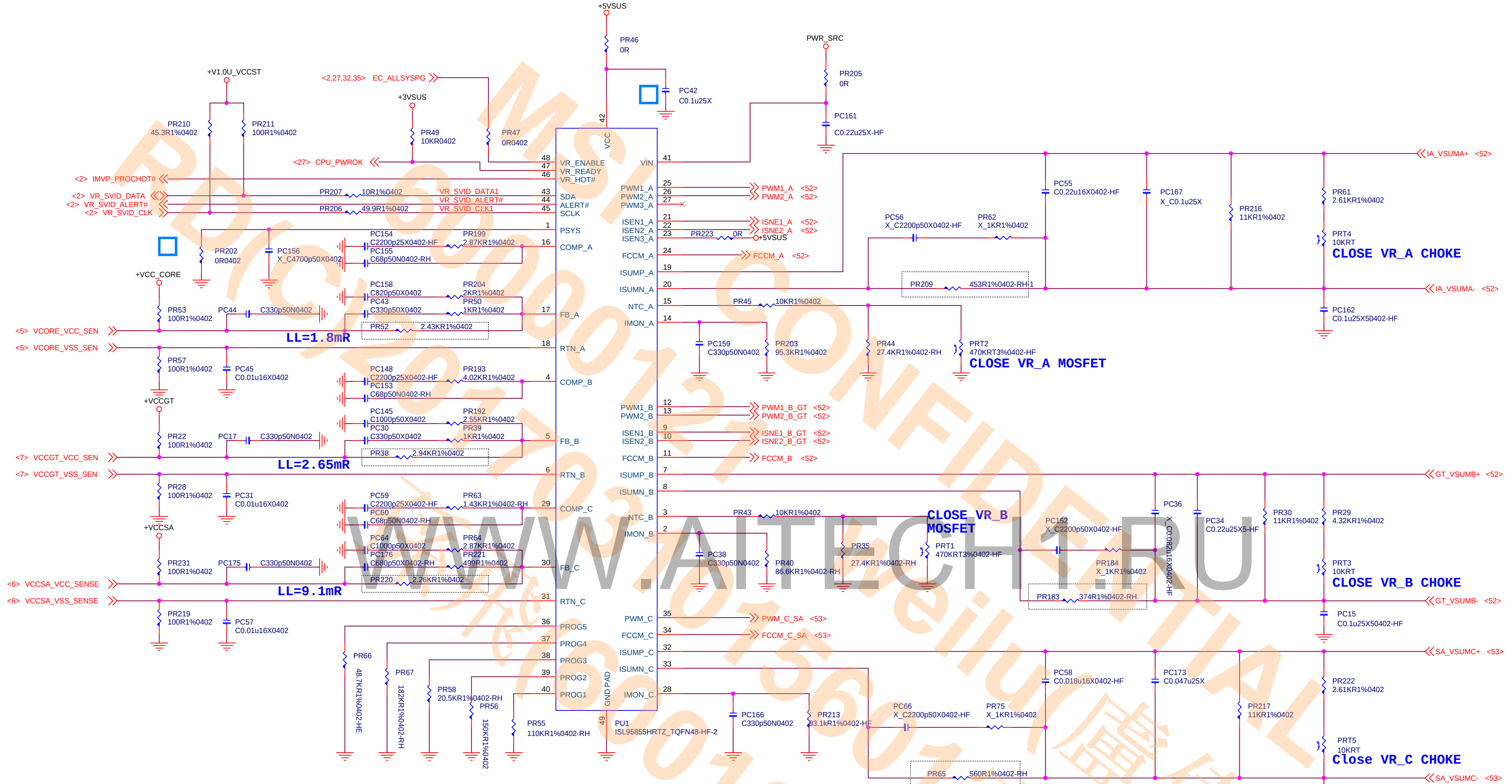
VBoot:0.8V

Vmin:0.5V / Vmax:1.25V



msi MICRO-STAR INT'L CO.,LTD.		
Title: NVVDD PHASE 1~4		
Size	Document Number: MS-16J9	Rev: 0A
Date:	Sheet 50 of 62	

Skylake H-line 42 45W ISL95855



SKL-H(4+2)

PROG1	110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2	150KR	IMAX VR_A=70A, VR_A PSI1=1PH
PROG3	20.5KR	IMAX VR_B=60A, DROOP VR_B Active
PROG4	182KR	DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	48.7KR	IMAX VR_C=12A, Frequency=450kHz

msi MICRO-STAR INT'L CO.,LTD.

Title: Skylake CPU Power

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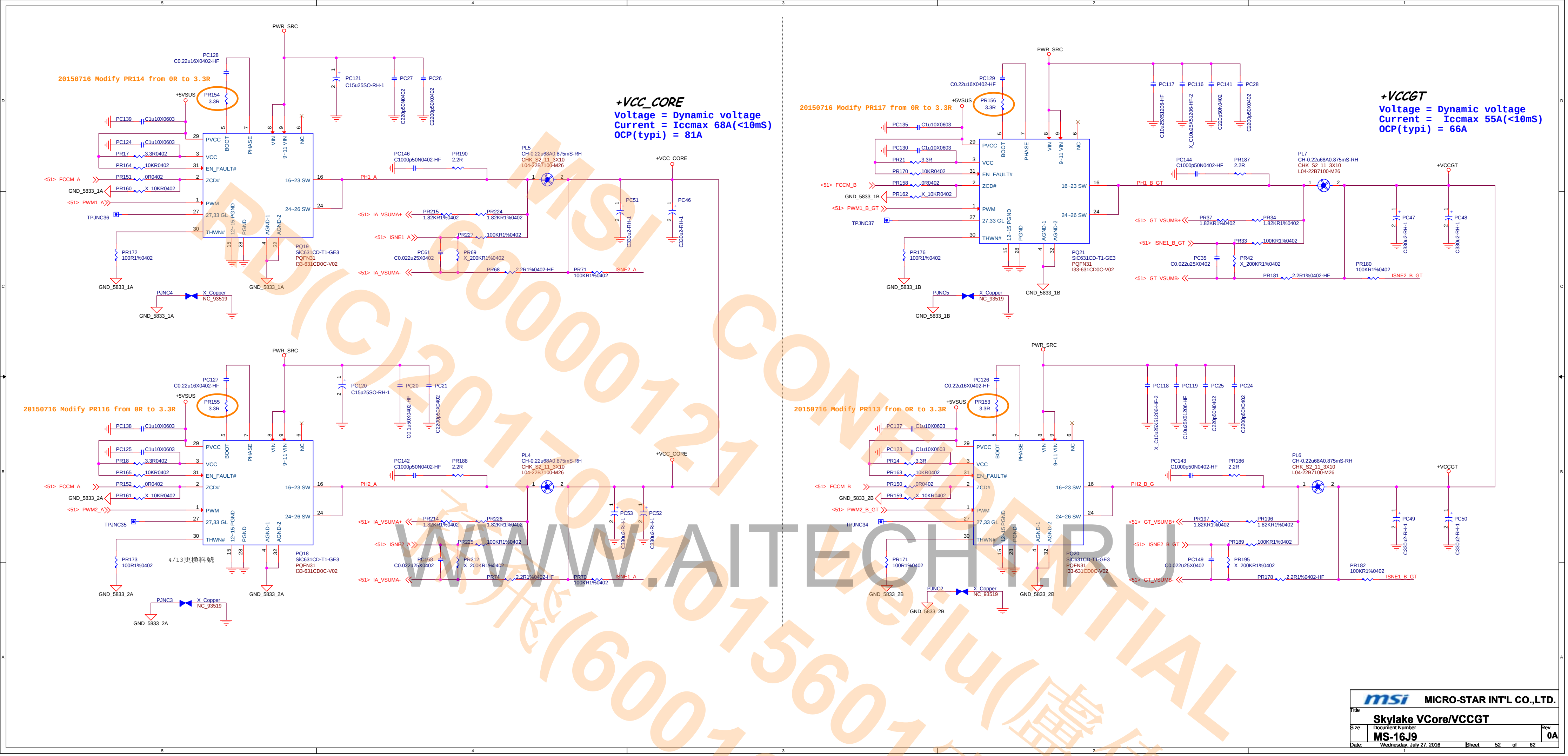

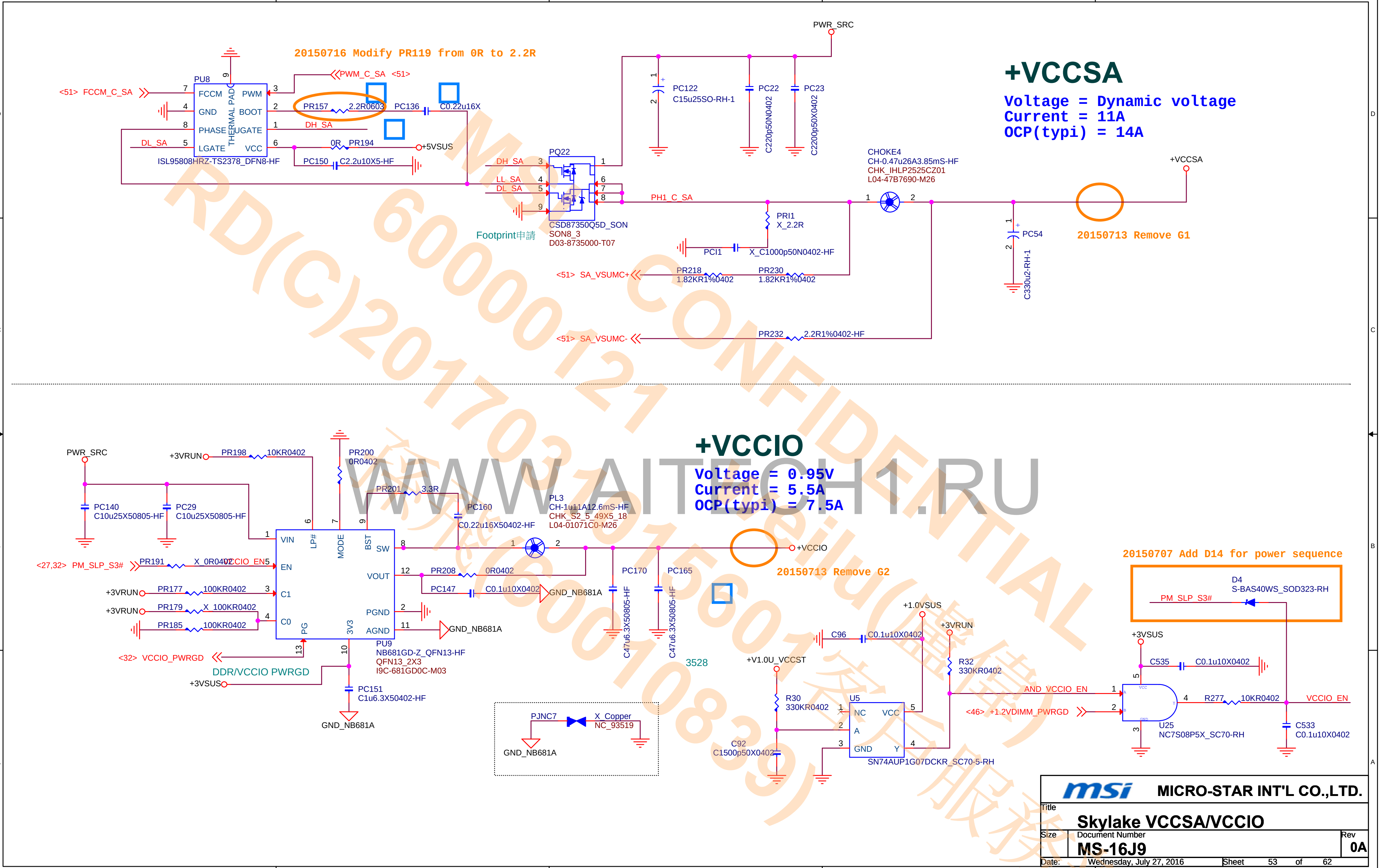

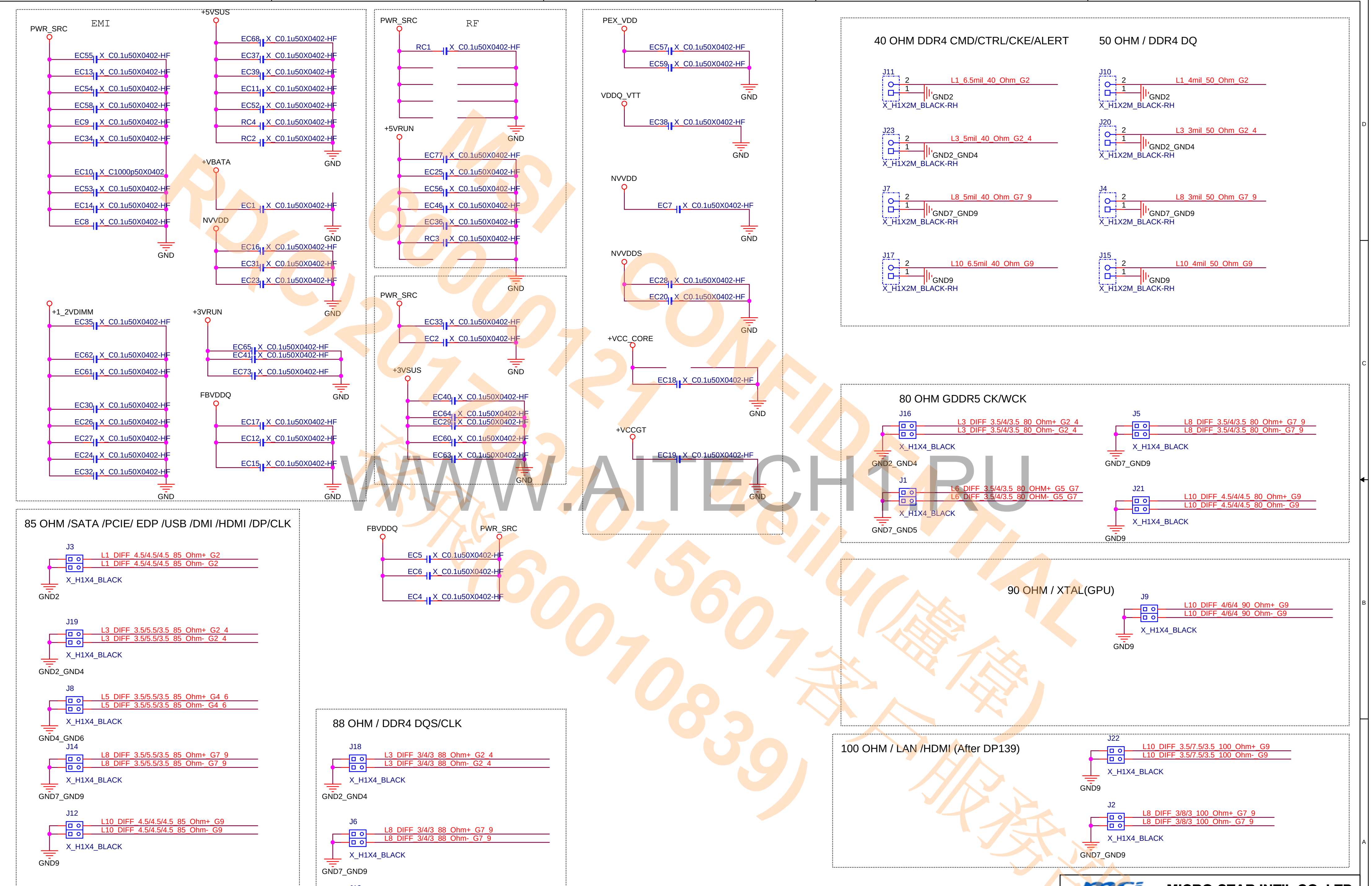

MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedance
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CPU/GPU Holes

MCPU4 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MCPU2 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MCPU3 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MCPU1 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MGPU2 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MGPU4 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MGPU1 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE
MGPU3 H_R276D169_PB_NH_R276D169_PB_N — GND X_CPU_HOLE

OD 2.3

MH7 H_R197D118_PT_N X_ME_SCREW HOLE
MH4 H_R197D118_PT_N X_ME_SCREW HOLE
修改內徑3mm
MH9 H_R197D91_N X_ME_SCREW HOLE
MH5 H_R197D91_N X_ME_SCREW HOLE
MH6 H_R197D91_N X_ME_SCREW HOLE

版邊 內3 / 外8

MH1 H_R197D118_PT_N X_ME_SCREW HOLE
HOLES_8X8_D3MM_VIA8_N MH8 X_8x8
MH3 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — GND
MH2 X_H_R197D118_PT_V3 H_R197D118_PT_V3 — LAN_GND

FM12 FM34 FM49 FM6 FM33 FM20 FM25 FM26
FM48 FM11 FM16 FM43 FM35 FM37 FM19 FM47
FM4 FM10 FM28 FM2 FM1 FM21 FM30 FM9
FM40 FM41 FM38 FM13 FM15 FM14
FM39 FM36 FM42 FM24
X_FM

4/13 新增

20150908 Un-stuff TP mylar UME16 for ME request
20150713 Add TP mylar UME16 for 16J4

Only 16J4

UME3	UME4	UME5	UME7	UME8	UME17	UME11	UME16
CPU BKT	GPU BKT	CPU MYLAR	LED SPONGE	LED SPONGE	ME_MYLAR	HIDE_GAP_ MYLAR	TP MYLAR
CPU BKT	GPU BKT	X_CPU MYLAR	LED SPONGE	LED SPONGE	Hide Caps Lock LED_MYLAR	X_HIDE_GAP_MYLAR	X_TP_MYLAR
E2M-7810111-A89	307-6H20211-C22	E2P-6J11211-Y42	E2Y-6J10611-Y42	E2Y-6J10611-Y42	E2Y-6324111-Y42	E2P-6J11411-Y42	E2Y-6J11811-G40

Only 1794

UME1	UME12	UME14	UME13	UME15	UME21
HDMI Lable	USB3_CON_ MYLAR	HDMI/DP MYLAR	MB MYLAR	SPONGE	MB MYLAR
HDMI ROYALTY	MYLAR	MYLAR	MB MYLAR	SPONGE	MB MYLAR
Y01-RHDMI03-000	E2M-3570611-Y42	E2M-3570611-Y42	E2P-7910311-G40	E2Y-7910211-G40	E2P-7910312-G40

HOLE10 NPTH_80 X_NPTH_80
HOLE11 NPTH_80 X_NPTH_80
HOLE7 H_NR118D118_1 X_H_NR118D118_1
HOLE6 H_NR118D118_1 X_H_NR118D118_1
HOLE2 npth_98 X_npth_98
HOLE13 npth_98 X_npth_98
HOLE12 npth_98 X_npth_98
HOLE1 npth_98 X_npth_98
HOLE15 X_NPTH_80 NPTH_80
HOLE4 X_NPTH_80 NPTH_80
HOLE3 X_NPTH_80 NPTH_80
HOLE8 X_NPTH_80 NPTH_80
HOLE5 X_NPTH_80 NPTH_80
HOLE14 X_NPTH_80 NPTH_80
HOLE9 X_NPTH_80 NPTH_80

PCB1 PD0-16J910B-H73 — PD0-16J910B-H73

UME2 BIOS Lable — BIOS_LABEL — G51-N1CO041-A09 For MP
UME20 ME_MYLAR — MYLAR — E2P-6J90111-G40

Top Spring

PAD6 X_HS-MS1011-RH ATE_C006_106 — E23-1011040-CA7
PAD2 X_HS-MS1011-RH ATE_C006_106
PAD3 X_HS-MS1011-RH ATE_C006_106
PAD4 X_HS-MS1011-RH ATE_C006_106
E23-1011040-CA7 E23-1011040-CA7 E23-1011040-CA7

BOT Spring

PAD1 X_HS-MS1011-RH ATE_C006_106
PAD5 X_HS-MS1011-RH ATE_C006_106
E23-1011040-CA7 E23-1011040-CA7

FM31 FM45 FM17 FM7 FM29 FM44 FM23 FM5
X_FM_NB2

MICRO-STAR INT'L CO.,LTD.
Title: Screw/ME
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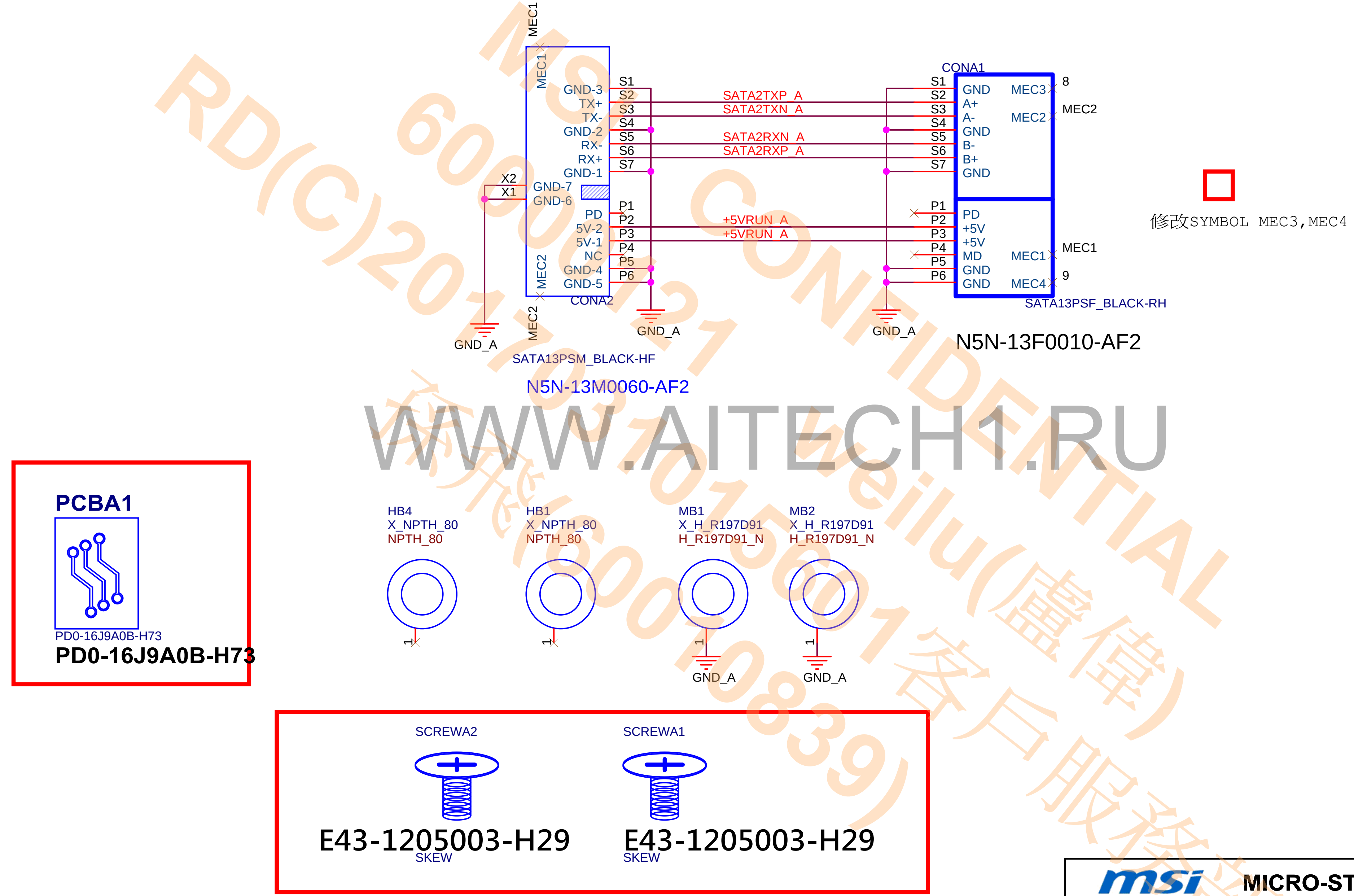
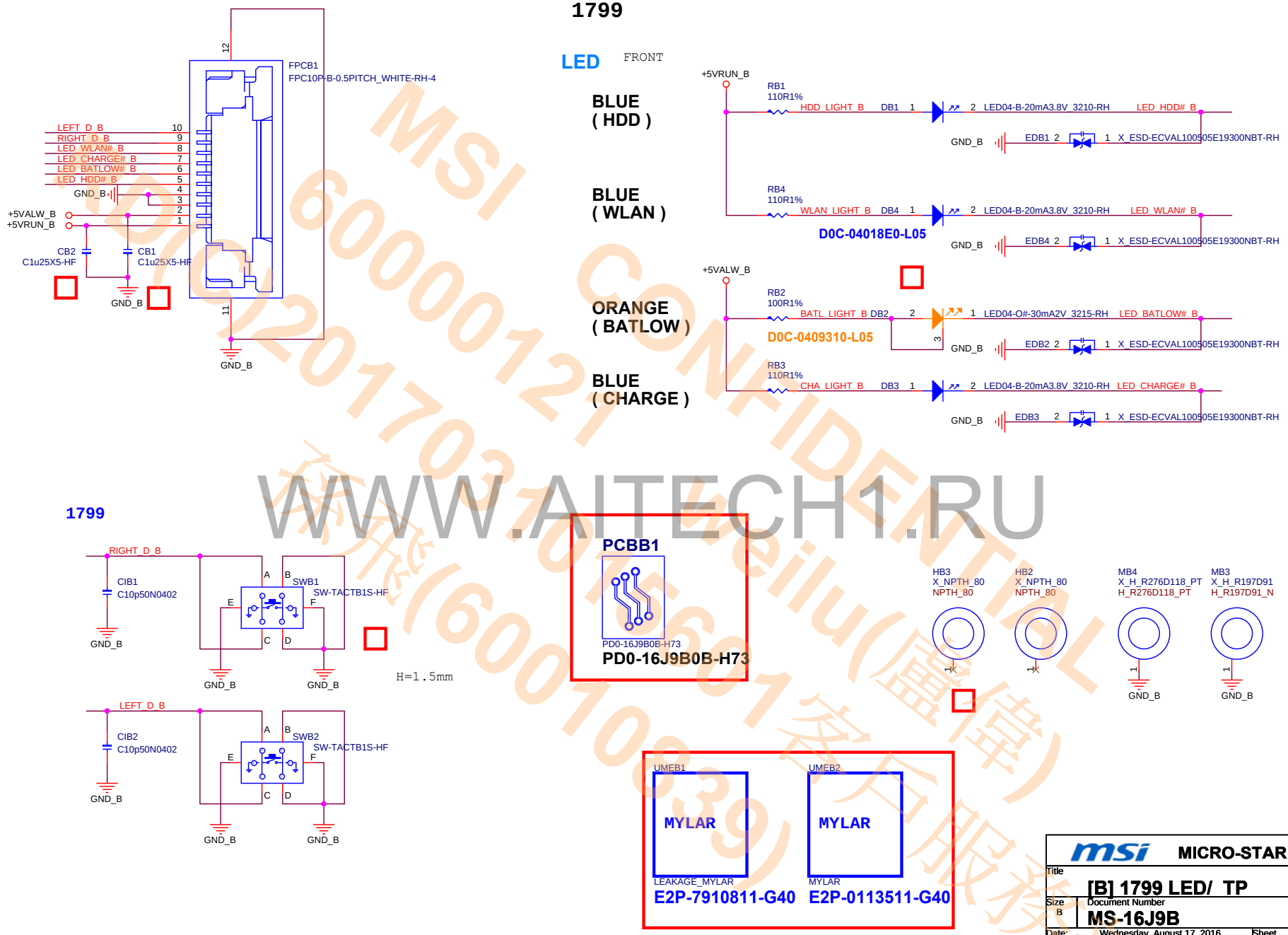


MICRO-STAR INT'L CO.,LTD.

Title: [A] 1799 ODD		
Size: A4	Document Number: MS-16J9A	Rev: 0A
Date: Wednesday, August 17, 2016	Sheet 56 of 62	



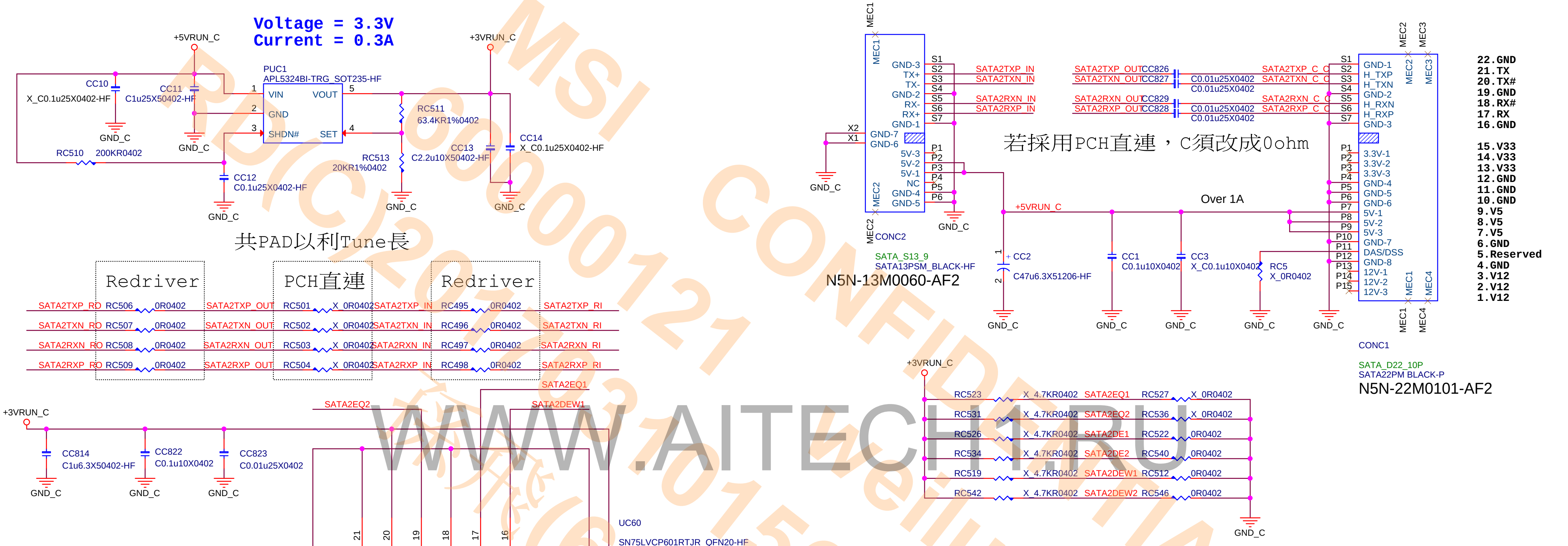
MICRO-STAR INT'L CO.,LTD.

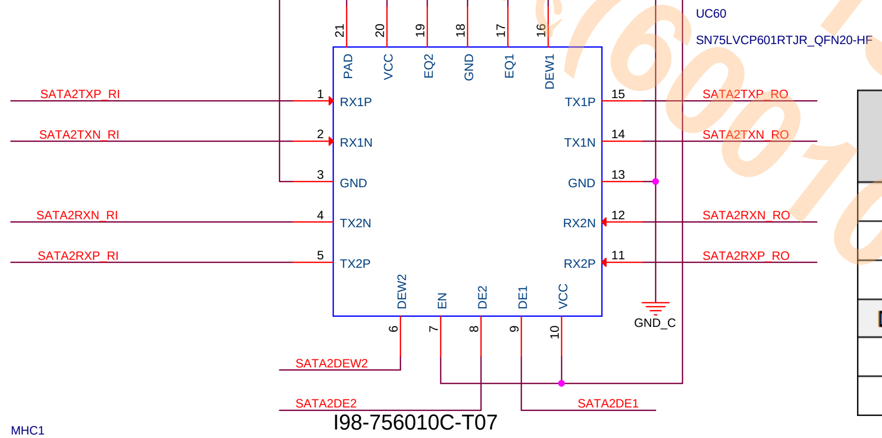
Title: [B] 1799 LED/ TP

Size: B | Document Number: MS-16J9B | Rev: 0A

Date: Wednesday, August 17, 2016 | Sheet 57 of 62

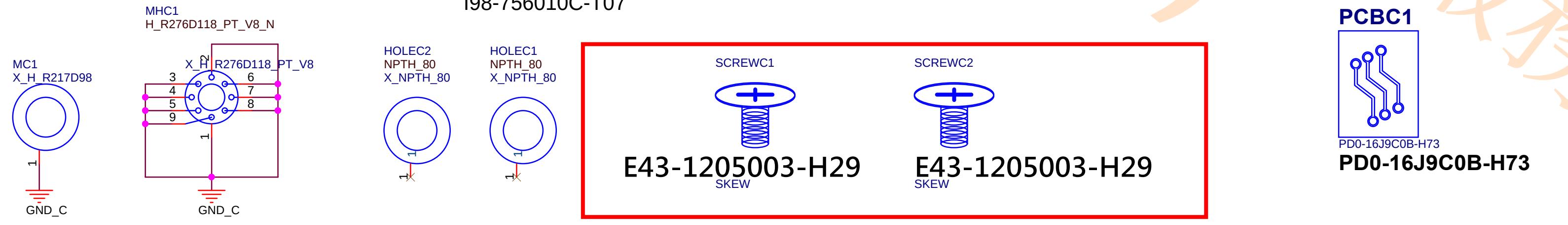
ODD SATA HDD





TX and RX EQ and DE Pulse-Duration Settings

DE1 OR DE2	CH1 OR CH2 DE-EMPHASIS dB (at 6 Gbps)	EQ1 OR EQ2	CH1 OR CH2 Equalization dB (at 6 Gbps)
NC (*default*)	–4	NC (*default*)	0
0	0	0	7
1	–2	1	14
DEW1 OR DEW2	**DEVICE FUNCTION → DE WIDTH FOR CH1/CH2**		
0	De-emphasis pulse duration, short		
1 (*default*)	De-emphasis pulse duration, long		



MICRO-STAR INT'L CO.,LTD.

Title: SATA ODD to HDD

Size: A3 | Document Number: MS-16J9C | Rev: 0A

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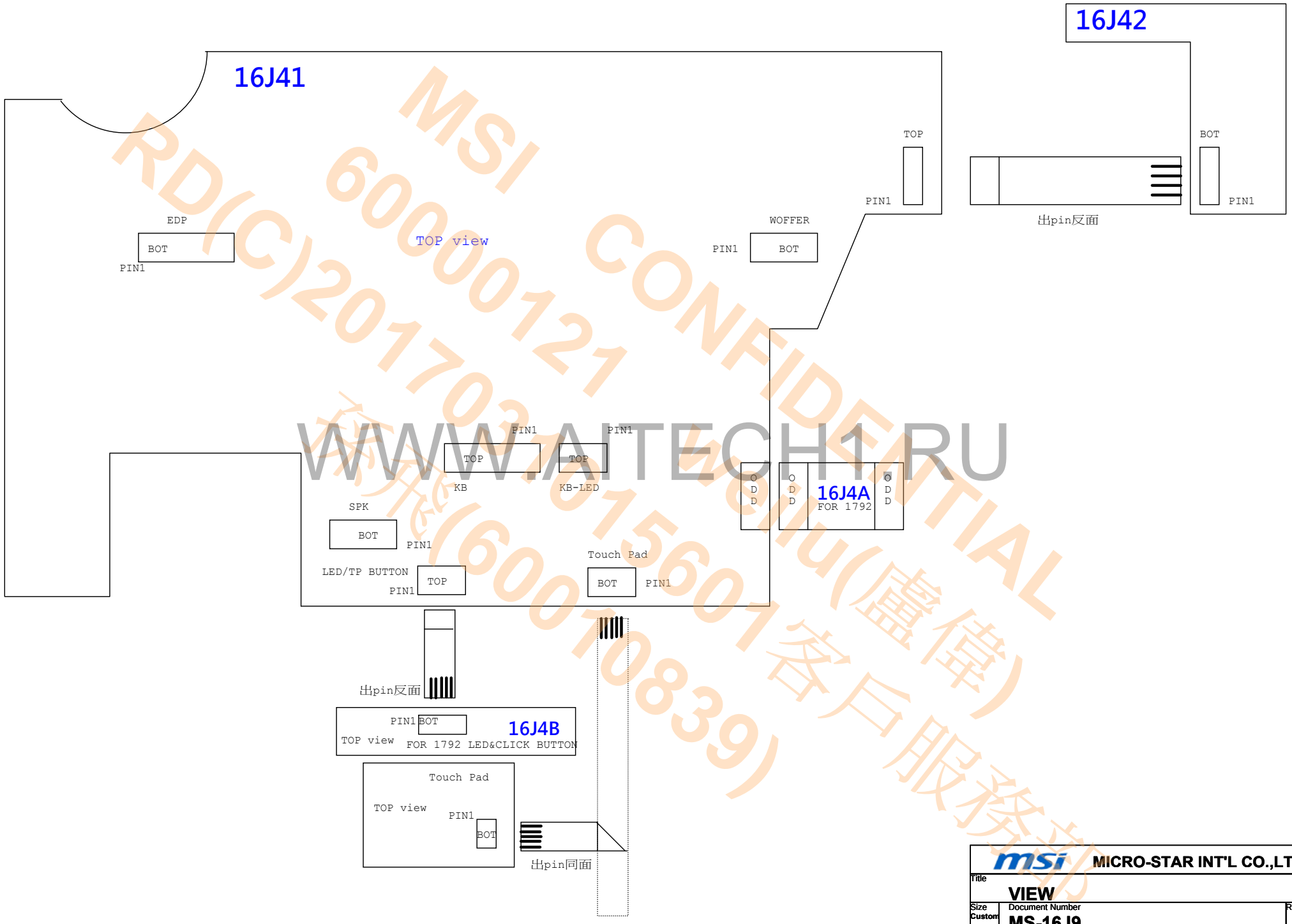


MICRO-STAR INT'L CO.,LTD.

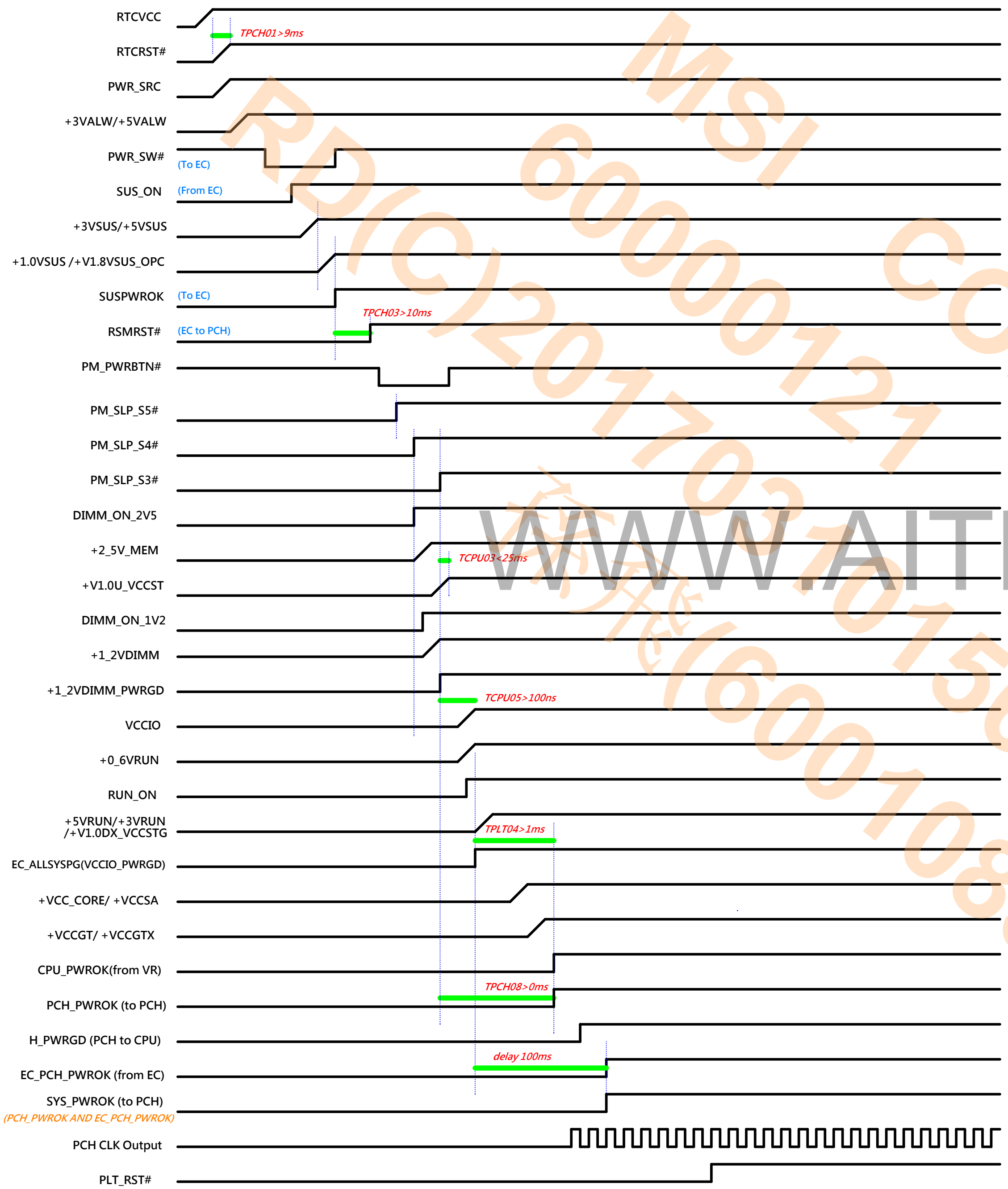
Title: VIEW

Size: Custom | Document Number: MS-16J9 | Rev: 0A

Date: Monday, May 30, 2016 | Sheet 59 of 62

Power on Sequence

G3 -> S0



MICRO-STAR INT'L CO.,LTD.

Title	Power on Sequence	
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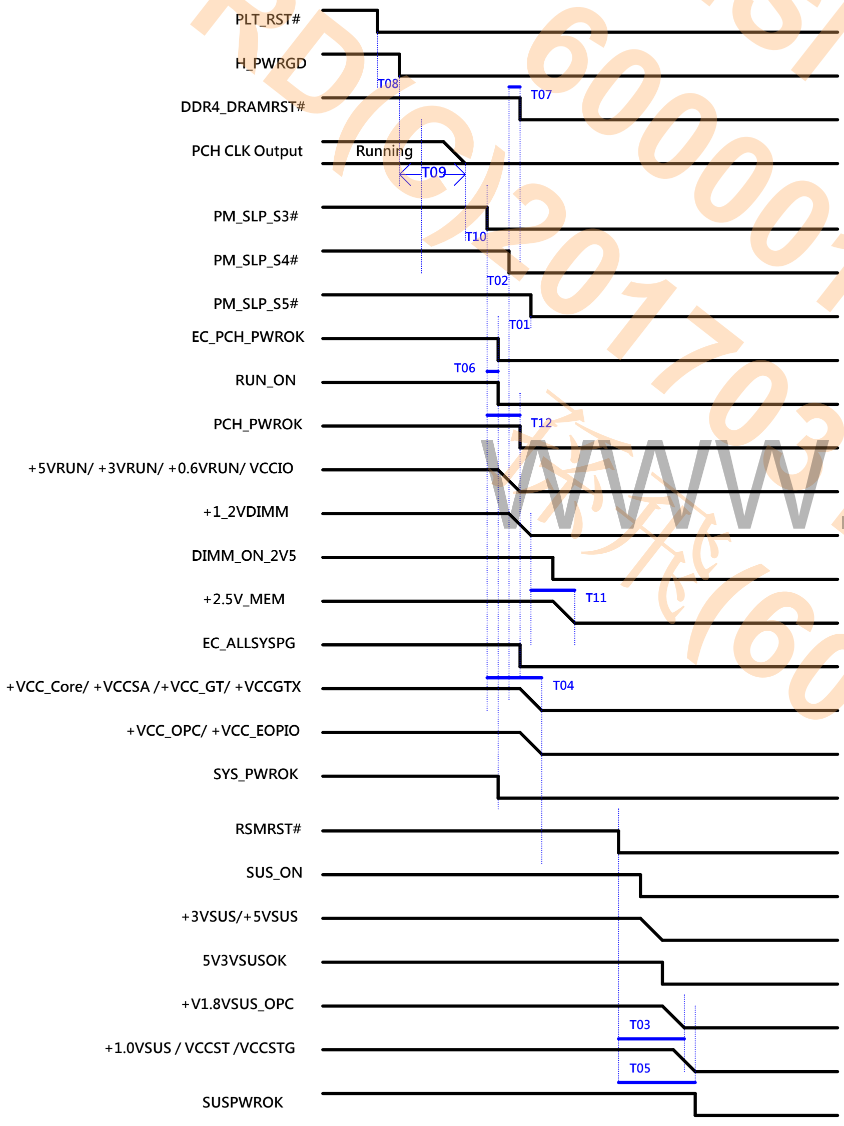
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

History

0A

Page	Description
28	REMOVE PU R164,R172,R151,R149
33	JNC13 CHANGE FOOTPRINT
	R176,R412 CHANGE TO JNC29,JNC30
30	ED10,ED11 PIN4,5 CHANGE NET
42	REMOVE G2
38	ADD ESD2
30	ADD TPS25810 U34 ED11 P/N SWAP
28	R144 PU TO 3VSUS
5	REMOVE R67
6	ADD C597
3	REMOVE R74,R72 ,C262
8	REMOVE C597
25	C646 CHANGE FOOTPRINT
	REMOVE R380 ,R376
31	DP REMOVE U8 ,ADD Q22,Q23,Q24
21	ADD R448 ,R380
30	ADD C725,C726
39	PR54,PC57 CHANGE FOOTPRINT
41	PC197 0805 CHANGE 0402 FOOTPRINT
42	PC91 0805 CHANGE 0402 FOOTPRINT
05	REMOVE R31
30	U34 CHANGE FOOTPRINT
29	REMOVE R139,R163
33	REMOVE C665 ADD JNC31
48	REMOVE J24 ,J17,J12,J18
49	REMOVE PAD1,PAD5,PAD9,PAD10
43	REMOVE G3,G4
48	ADD +1_2VDIMM EMI CAP
	REMOVE J19,J22
42	ADD PC666

0A

Page	Description	Date
12~17 19~21	memory change RC料號統一	5/12
27	Change R111 reference 4.99K to 20K	5/13
30	D3 +3VRUN change to 3V_NV	
49	PR61 :1ohm 0402 >0603 (R11-0010023-W08) PC64 :1u 0402>0603 (C11-1057613-W08) PR74 :205Kohm>187Kohm(R11-1873T12-W08)	5/14
52	+1VSUS VCC分壓	
33	U17 CPU_POWOK add C to ground	5/15
49	PR33換料	
44	CON10 Change to N54-06F1371-SL0 CN13 Change to N58-08F0191-SL0	5/18
39	Y4 change to D04-0901000-SC6	
	R190 改不上件	
37	LED限流電阻改值	
54	PC62 change to C11-4722812-M09	
	1VSUS PR223 : 12.4K?13K(R11-0133T12-W08) DIMM PU5 : APW8819?TPS51216 (I32-512160C-T07) PR91 : 110K?150K(R11-0154T12-W08) PR219,PC200 : NC?上件 FBVDDQ PR7,CI1 : NC?上件 VCORE PR174 : 499R?470R(R11-0471T12-W08) PR164 : 95.3K?82K(R11-0823T12-W08) PR34 : 2.43K?2.15K(R11-2151T12-W08) PR32 : 499R?1K(R11-0102T12-W08) PR160 : 1.4K?2.87K(R11-2871T12-W08) PR109,PR110 : NC?0R(R11-0000012-W08) PR123,PR122 : 10K?NC PR51,PR175 : 200k?NC PC163 : 0.22u?0.1u(C11-1042023-Y01) PC48 : 0.082u?0.1u(C11-1042812-Y01) PC154 : 680p?820P(C11-8212012-W08) PC36 : 680p?330P(C11-3312012-W08) VGT PR144 : 412R?340R(R11-0341T12-W08) PR14 : 2.61K?4.32K(R11-4321T12-W08) PR24 : 97.6K?86.6K(R11-8662T12-W08) PR154 : 2K?2.55K(R11-2551T12-W08) PR23 : 499R?1K(R11-0102T12-W08) PR155 : 1K?4.02K(R11-4021T12-W08) PR120,PR108 : NC?0R(R11-0000012-W08) PR124,PR121 : 10K?NC PR25,PR157 : 200k?NC PC22 : 680p?330P(C11-3312012-W08) PC139 : 680p?1000P(C11-1022012-W08) VCCSA PR45 : 619R?560R(R11-0561T12-W08) PR182 : 2.15K?2.26K(R11-2261T12-W08) PR176 : 100K?91K(R11-0913T12-W08) PR44 : 2K?2.87K(R11-2871T12-W08) PC168 : 0.068u?0.047u(C11-4732043-Y01) PC51 : 0.082u?6800P(C11-6822612-W08) PC56 : 680p?1000P(C11-1022012-W08)	5/20
26	Y6 change to D04-1103510-F07 PC24,38,50 : 0.01uF change to C11-1032012-W08	5/25
54	Add UMEB1 , UMEB2	5/29
	PU2 change to I32-958552C-I11	
	CPU change to OAD-14A1001	
	PCH change to OB1-14A1001	
	U12 change to I36-258100C-T07	

10

Page	Description	Date
	R247 ,R441,D8stuff R147,R464,R448上件 U39 change to B07-F021J44-EB3 U43 change to M31-25B6412-GA0 U13 change to B02-011422C-AD0	6/12
	VCORE: PR174 : 470R'453R(R11-4530T22-W08) PR34 : 2.15K'2.43K(R11-2431T12-W08) PC163 : 0.1u?NC PC48 : 0.1u'0.22u(C11-2242512-M09) PR164 : 82K'95.3K(R11-9532T12-W08) FBVDDQ PR11 : 33.2K?27K(R11-2702T12-W08) VGT: PR144 : 340R'374R(R11-3740T12-W08) VCCSA: PC51 : 6800P'0.018u (C11-1832512-M09) PR176 : 91K'93.1K(R11-9312T12-W08)	6/16
	PR147,PR150,PR151,PR152 PC135,PC136,PC137,PC138 上件 R72 change to L02-1008023-T19	6/17
	U29 change to N-90-GSMS1-RH	6/22
	ED10, ED11 stuff	6/23
	E207不上 R219上件	
	CPU PC105,PC106,PC107,PC108,PC109,PC110,PC112,PC113, DGPU : PC167,PC169,PC170,PC178,PC183,PC184,PC185,PC187 Change to C11-1067610-M09	6/24
	E2P-6J11211-Y42移除	6/25
	Add E2Y-Z001711-G40*2	
	Add BIOS Socket	

Page	Description	Date
43	Change R421 from 33R to 22R	7/7
43	Change C413 & C414 from 20p to 33p	
51	Change R135 from 0R to 4.7KR Add D13 circuit for power sequence	
57	Add D14 circuit for power sequence	
59	Stuff UME2	
	Remove all gate	7/13
59	Add UME16 for 16J4 TP Mylar	
54	Modify PR79 & PR194 from 2.2R to 2.7R	7/16
56	Modify PR114 & PR116 & PR113 & PR117 from 0R to 3.3R	
57	Modify PR119 from 0R to 2.2R	
60	Unstuff A board component for 16J4	
61	Unstuff B board component for 16J4	
36	Stuff UB1 & unstuff UB2 for 1794	7/24
40	20150724 Modify F1 location	
34	20150727 Remove BIOS ROM sucket	7/27
38	20150727 Remove SW3 & C207	
	Modify to 1.0 BOM	8/6
	Change CPU PN to A0D-6700H15-I06 PCH PN to B01-HM17005-I06	8/12
	Change R348 from 20KR to 4.7KR	
38	Unstuff CON6	8/17
	Change BIOS label to G51-N1C0041-A09 for AMI	8/18
	Change 2N7002 dual PN to D03-65D8L09-D07 for Safety	
	Change UME11 to un-stuff for ME request	8/24
	Modify DGPU VRAM size from 3G to 6G and strap value	9/03
	Change UME16 to un-stuff for ME request	9/08
	Modify GPU HW strap value to correct	11/30

MICRO-STAR INT'L CO.,LTD.

Title: History

Size | Document Number: MS-16J9 | Rev: 0A

Date: Monday, May 30, 2016 | Sheet 62 of 62